

# SUPERO<sup>®</sup>

SUPER P3TDE6  
SUPER P3TDER

## USER'S MANUAL

Revision 1.0c

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## Preface

### About This Manual

This manual is written for system integrators, PC technicians and knowledgeable PC users. It provides information for the installation and use of the SUPER P3TDE6/P3TDER mainboard. The SUPER P3TDE6/P3TDER support single or dual Pentium® III 500 MHz-1.40 GHz FCPGA processors with a 512K L2 cache at a 133/100 MHz front side bus. Please refer to the support section of our web site (<http://www.supermicro.com/TechSupport.htm>) for a complete listing of supported processors.

Pentium III FCPGA (Flip Chip Pin Grid Array) processors are housed in a 370-pin socket, which is the standard that will support future Intel processors. The P3TDER has been optimized for use in 1U rackmount systems.

### Manual Organization

**Chapter 1** includes a checklist of what should be included in your mainboard box, describes the features, specifications and performance of the SUPER P3TDE6/P3TDER mainboard and provides detailed information about the chipset.

**Chapter 2** begins with instructions on handling static-sensitive devices. Read this chapter when you want to install the processor and DIMM memory modules and when mounting the mainboard in the chassis. Also refer to this chapter to connect the floppy and hard disk drives, SCSI drives, the IDE interfaces, the parallel and serial ports and the twisted wires for the power supply, the reset button, the power LED, the speaker and the keyboard.

**Chapter 3** describes troubleshooting procedures for the video, the memory and the setup configuration stored in CMOS. For quick reference, a general FAQ section is provided. Instructions are also included for contacting technical support. In addition, you can visit our web site at [www.supermicro.com/techsupport.htm](http://www.supermicro.com/techsupport.htm) for more detailed information.

**Chapter 4** includes an introduction to BIOS and provides detailed information on running the CMOS Setup utility.

**Appendix A** gives information on BIOS error beep codes.

**Appendix B** provides POST checkpoint codes.

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# Chapter 1

## Introduction

### 1-1 Overview

#### Checklist

Congratulations on purchasing your computer motherboard from an acknowledged leader in the industry. Supermicro boards are designed with the utmost attention to detail to provide you with the highest standards in quality and performance.

Please check that the following items have all been included with your motherboard. If anything listed here is damaged or missing, contact your retailer.

One (1) Supermicro Mainboard

One (1) ribbon cable for IDE devices

One (1) floppy ribbon cable for  
(a) 5.25-inch floppy and  
(b) 3.5-inch floppy drives

One (1) I/O backpanel shield

One (1) Supermicro CD or diskettes containing drivers and utilities

One (1) User's/BIOS Manual

SCSI Accessories (P3TDE6 only)

One (1) 50-pin Ultra SCSI cable

One (1) 68-pin LVD SCSI cable

One (1) set of SCSI driver diskettes

One (1) SCSI manual

## Contacting Supermicro

### Headquarters

Address: Super Micro Computer, Inc.  
980 Rock Ave.  
San Jose, CA 95131 U.S.A.

Tel: +1 (408) 503-8000

Fax: +1 (408) 503-8008

Email: [marketing@supermicro.com](mailto:marketing@supermicro.com) (General Information)  
[support@supermicro.com](mailto:support@supermicro.com) (Technical Support)

Web Site: [www.supermicro.com](http://www.supermicro.com)

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[support@supermicro.nl](mailto:support@supermicro.nl) (Technical Support)  
[rma@supermicro.nl](mailto:rma@supermicro.nl) (Customer Support)

### Asia-Pacific

Address: 3F, #753 Chung-Cheng Road  
Chung-Ho City, Taipei Hsien, Taiwan, R.O.C.

Tel: +886-(2) 8228-1366

Fax: +886-(2) 8221-2790

Web Site: [www.supermicro.com.tw](http://www.supermicro.com.tw)

Technical Support:

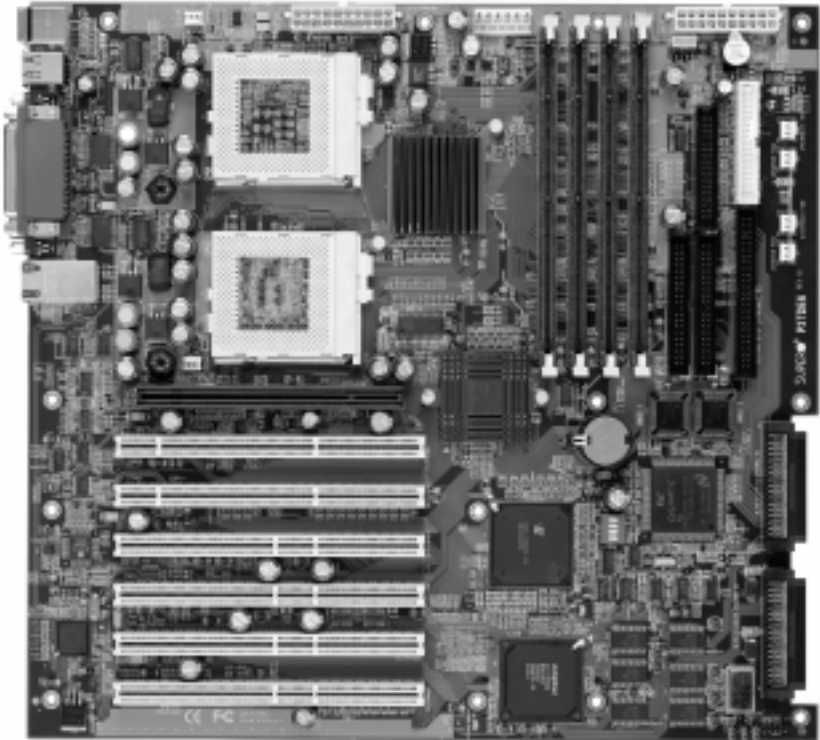
Email: [support@supermicro.com.tw](mailto:support@supermicro.com.tw)

Tel: 886-2-8228-1366, ext.132 or 139

## Notes

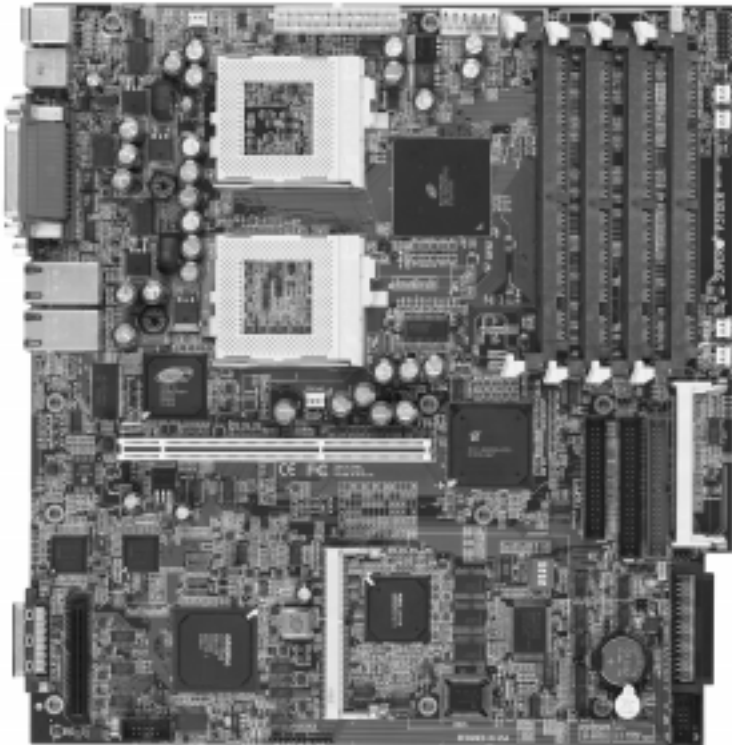
## SUPER P3TDE6

Figure 1-1. SUPER P3TDE6 Image

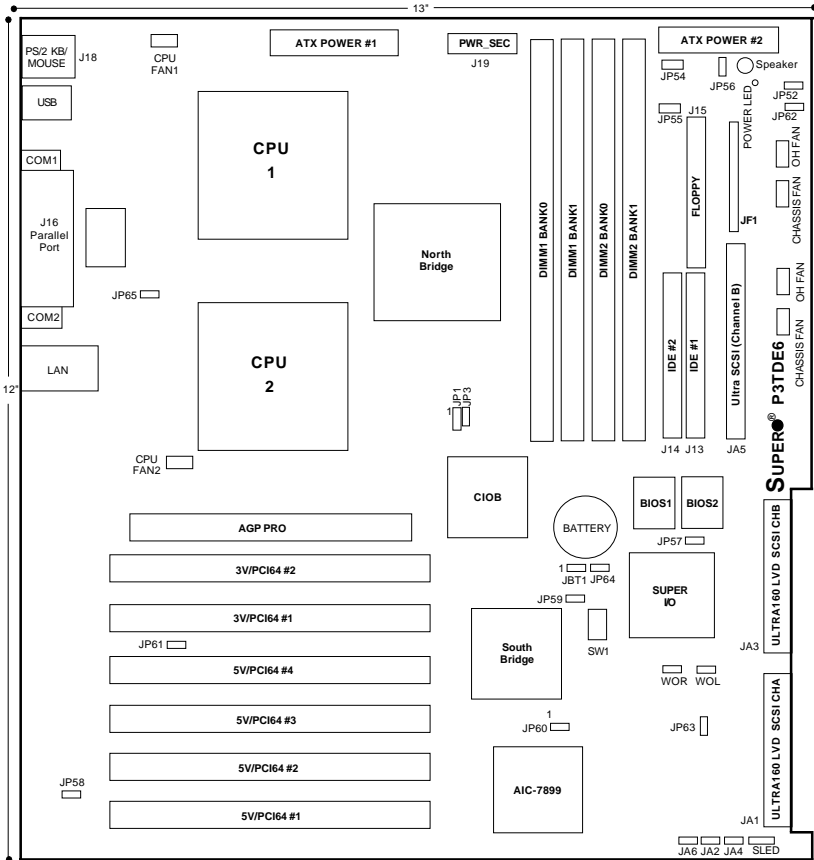


## SUPER P3TDER

Figure 1-2. SUPER P3TDER Image



**Figure 1-3. SUPER P3TDE6 Layout**  
(not drawn to scale)



Note: Memory modules must be installed in pairs.  
DIP Switch 1 sets the CPU speed.

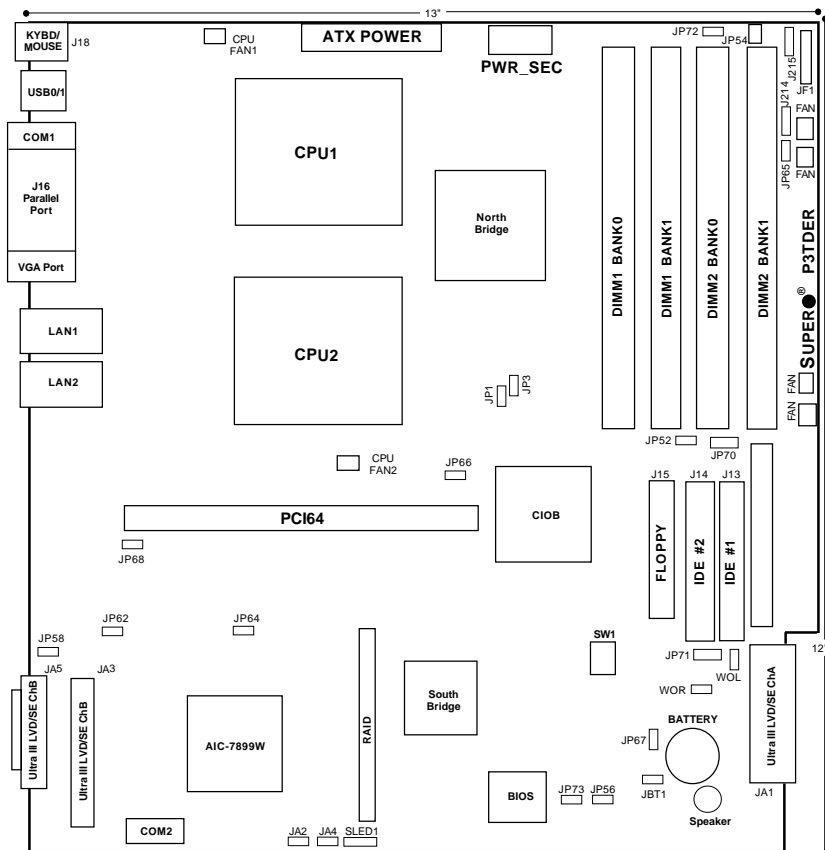
Also see Chapter 2 for the locations of the I/O ports and Front Control Panel (JF1) connectors and for details on jumper settings and pin definitions.

## P3TDE6 Quick Reference

<b><u>Jumper</u></b>	<b><u>Description</u></b>	<b><u>Default Setting</u></b>
JA2	LVD SCSI Ch A Term.	Open (Enabled)
JA4	LVD SCSI Ch B Term.	Open (Enabled)
JA6	50pin SCSI Ch B Term	Open (Enabled)
JBT1	CMOS Clear	Pins 1-2 (Normal)
JP1	FSB Speed Setting	Pins 1-2 (Auto)
JP3	Spread Spectrum	Open (Disabled)
JP55	Third P/S Fail Enable/Disable	Open (Disabled)
JP56	Speaker Enable/Disable	Closed (Enabled)
JP57	BIOS Select	Pins 1-2 (BIOS1)
JP58	LAN/NIC Enable/Disable	Open(Enabled)
JP60	SCSI Enable/Disable	Pins 1-2 (Enabled)
JP61	PCI 66/33 MHz Select	Open (66 MHz)
JP62	Thermal Fan Enable/Disable	Closed (Enabled)
JP64	Watchdog Enable/Disable	Open (Disabled)
JP65	CPU/CPU Chassis Fan Select	Closed (CPU Fan)

<b><u>Connector</u></b>	<b><u>Description</u></b>
ATX POWER #1	Primary ATX Power Connector
ATX POWER #2	Secondary ATX Power Connector
BANK0-BANK1	Memory (RAM) Slots
COM1/COM2	COM1/COM2 Serial Port Connector
CPU1/CPU2	CPU 1 and CPU2 Sockets
CPU/CH/OH FAN	CPU/Chassis/Overheat Fan Headers
J13, J14	IDE Hard Disk Drive Connectors
J15	Floppy Disk Drive Connector
J16	Parallel Printer Port
J18	PS/2 Keyboard/Mouse Ports
JA1	Ultra160 LVD SCSI CH A Connector
JA3	Ultra160 LVD SCSI CH B Connector
JF1	Front Control Panel Connector
JP52	Chassis Intrusion Header
JP54	Third Power Supply Fail Header
JP63	NMI (Non-Maskable Interrupt) Connector
LAN	Ethernet Port
PWR_SEC	Secondary ATX Power Connector
SLED1	SCSI Active LED Header
USB	Universal Serial Bus Ports
WOL	Wake-on-LAN Header
WOR	Wake-on-Ring Header

**Figure 1-4. SUPER P3TDER Layout**  
(not drawn to scale)



Note: Memory modules must be installed in pairs.  
DIP Switch 1 sets the CPU speed.

Also see Chapter 2 for the locations of the I/O ports and Front Control Panel (JF1) connectors and for details on jumper settings and pin definitions.

## P3TDER Quick Reference

<b><u>Jumper</u></b>	<b><u>Description</u></b>	<b><u>Default Setting</u></b>
JA2	LVD SCSI Ch A Term.	Open (Enabled)
JA4	LVD SCSI Ch B Term.	Open (Enabled)
JBT1	CMOS Clear	Pins 1-2 (Normal)
JP1	FSB Speed Setting	Pins 1-2 (Auto)
JP3	Spread Spectrum	Open (Disabled)
JP56	Speaker Enable/Disable	Closed (Enabled)
JP58	LAN1 Enable/Disable	Pins 1-2 (Enabled)
JP62	LAN2 Enable/Disable	Pins 1-2 (Enabled)
JP64	SCSI Enable/Disable	Pins 1-2 (Enabled)
JP65	Thermal Fan On/Off	Open (Off)
JP68	VGA Enable/Disable	Pins 1-2 (Enabled)
JP72	CPU/CPU Chassis Fan Select	Closed (CPU Fan)
JP73	Watchdog Enable/Disable	Open (Disabled)

<b><u>Connector</u></b>	<b><u>Description</u></b>
ATX POWER	Primary ATX Power Connector
BANK0/BANK1	Memory (RAM) Slots
COM1/COM2	COM1/2 Serial Port Connector/Header
CPU/CH/OH FAN	CPU/Overheat/Chassis Fan Headers
J13, J14	IDE Hard Disk Drive Connectors
J15	Floppy Disk Drive Connector
J16	Parallel Printer Port
J18	PS/2 Keyboard/Mouse
J214	USB3 Header
J215	Power LED Header
JA1	Ultra160 Channel A LVD SCSI
JA3	Ultra160 Channel B LVD SCSI
JF1	Front Control Panel
JP52	Chassis Intrusion Header
JP54	Third Power Supply Fail Header
JP67	NMI (Non-Maskable Interrupt) Connection
JP70	IPMB Connector
JP71	SMB Connector
LAN1/LAN2	Ethernet Port 1 / Ethernet Port 2
PWR_SEC	Secondary ATX Power Connector
RAID	RAID Port Connector
SLED1	SCSI Active LED Header
USB 0/1	Universal Serial Bus Ports
WOL	Wake-on-LAN Header
WOR	Wake-on-Ring Header

## Motherboard Features

### CPU

- Single or dual Pentium® III FCPGA 500 MHz-1.40 GHz FCPGA processors with a 512K L2 cache at front bus speeds of 133 and 100 MHz.

**Note:** Please refer to the support section of our web site for a complete listing of supported processors (<http://www.supermicro.com/TechSupport.htm>). You must use the server version of the processors mentioned above.

### Memory

- Four 168-pin DIMM sockets supporting up to 4 GB of registered ECC SDRAM

**Note:** The memory speed must match the front side bus speed being used. (Both 133 or 100 MHz.) Also, memory modules must be installed in pairs (first in the two slots of Bank0, then in both slots of Bank1, if needed).

### Chipset

- ServerWorks ServerSet III HE Super Light

### Expansion Slots

#### P3TDE6:

- Two 64-bit, 66/33 MHz PCI slots
- Four 64-bit, 33 MHz PCI slots
- One 2x/AGP Pro (ATI 8 MB Rage Graphics Card included)

#### P3TDER:

- One 64-bit, 66/33 MHz PCI

### BIOS

- 4 Mb AMI® Flash ROM
- APM 1.2, DMI 2.1, PCI 2.2, ACPI 1.0, Plug and Play (PnP)

### PC Health Monitoring

- Seven onboard voltage monitors for CPU core, chipset voltage, +5V and +12V
- Fan status monitor with firmware/software on/off control
- Environmental temperature monitor and control
- CPU fan auto-off in sleep mode
- Power-up mode control for recovery from AC power loss
- System overheat LED and control
- System resource alert

### **ACPI/PC 98 Features**

- Microsoft OnNow
- Slow blinking LED for suspend state indicator
- Main switch override mechanism
- External modem ring-on

### **Onboard I/O**

- AIC-7899 for dual channel Ultra160 SCSI
- ATI Rage 8 MB Graphics Card (P3TDE6)
- Integrated ATI Rage XL Graphics Controller (P3TDER)
- Intel 82559 for integrated onboard Ethernet
  - 1 Ethernet port (P3TDE6)
  - 2 Ethernet ports (P3TDER)
- 2 EIDE bus master interfaces support Ultra DMA/33 (P3TDE6)
- 2 EIDE bus master interfaces support Ultra DMA/100 (P3TDER)
- 1 floppy port interface (up to 2.88 MB)
- 2 Fast UART 16550A compatible serial ports
- 1 EPP/ECP (Enhanced Parallel Port/Extended Capabilities Port)
- PS/2 mouse and PS/2 keyboard ports
- 2 USB (Universal Serial Bus) ports

### **Other**

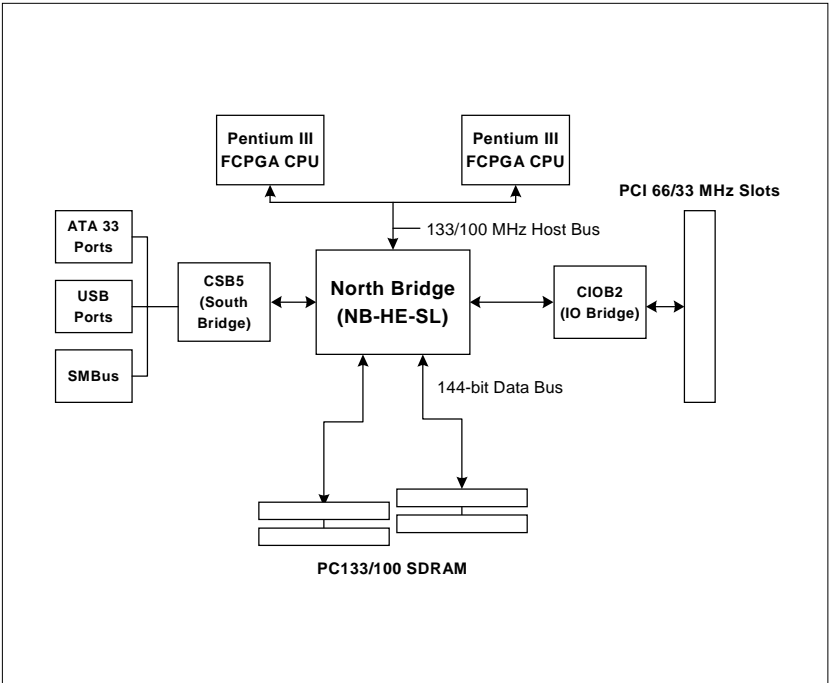
- Internal/external modem ring-on
- Recovery from AC power loss control
- Wake-on-LAN (WOL)

### **CD/Diskette Utilities**

- BIOS flash upgrade utility
- Device Drivers

### **Dimensions**

- SUPER P3TDE6
  - Extended ATX: 12.05" x 13" (306 x 330 mm)
- SUPER P3TDER
  - Full ATX: 12.05" x 11.475" (306 x 291 mm)



**Figure 1-5. ServerWorks HE-SL Chipset:  
System Block Diagram**

**Note:** This is a general block diagram. Please see the previous Motherboard Features Section for details on the features of each motherboard.

## 1-2 Chipset Overview

The ServerWorks ServerSet™ III HE SL is a high-performance core logic chipset that consists of a North Bridge and a South Bridge.

The North Bridge integrates the main memory subsystem and a dual channel PCI bus and bridges the processor bus to a 64-bit PCI bus. The memory subsystem consists of a two-way interleaved 4-DIMM configuration accessed over a 144-bit memory bus (most chipsets have a 72-bit memory bus), which provides a significant boost in performance. The North Bridge also packs and unpacks data for PCI accesses to reserve more processor bandwidth for multiprocessor motherboards.

The South Bridge provides various integrated functions, including the PCI to ISA bridge and support for UDMA33, security (passwords and system protection), Plug & Play, USBs, power management, interrupt controllers and the SMBus.

## 1-3 Special Features

### **ATI Graphics Controller (P3TDER only)**

The P3TDER has an integrated ATI video controller based on the Rage XL graphics chip. The Rage XL fully supports sideband addressing and AGP texturing. This onboard graphics package can provide a bandwidth of up to 512 MB/sec over a 32-bit graphics memory bus.

### **BIOS Recovery**

The BIOS Recovery function allows you to recover your BIOS image file if the BIOS flashing procedure fails (see Section 3-3).

### **Recovery from AC Power Loss**

BIOS provides a setting for you to determine how the system will respond when AC power is lost and then restored to the system. You can choose for the system to remain powered off (in which case you must hit the power switch to turn it back on) or for it to automatically return to a power on state. See the Power Lost Control setting in the Advanced BIOS Setup section (Peripheral Device Configuration) to change this setting. The default setting is Always On.

## 1-4 PC Health Monitoring

This section describes the PC health monitoring features of the SUPER P3TDE6/P3TDER. These motherboards have an onboard System Hardware Monitor chip that supports PC health monitoring.

### **Onboard Voltage Monitors for the CPU Core, Chipset Voltage, +5V and +12V**

The onboard voltage monitor will scan these voltages continuously. The +3.3V level is also monitored. Once a voltage becomes unstable, a warning is given or an error message is sent to the screen. Users can adjust the voltage thresholds to define the sensitivity of the voltage monitor.

### **Fan Status Monitor with Firmware/Software On/Off Control**

The PC health monitor can check the RPM status of the cooling fans. The onboard 3-pin CPU and chassis fans are controlled by the power management functions. The thermal fan is controlled by the overheat detection logic.

### **Environmental Temperature Control**

The thermal control sensor monitors the CPU temperature in real time and will turn on the thermal control fan whenever the CPU temperature exceeds a user-defined threshold. The overheat circuitry runs independently from the CPU. It can continue to monitor for overheat conditions even when the CPU is in sleep mode. Once it detects that the CPU temperature is too high, it will automatically turn on the thermal control fan to prevent any overheat damage to the CPU. The onboard chassis thermal circuitry can monitor the overall system temperature and alert users when the chassis temperature is too high.

### **CPU Fan Auto-Off in Sleep Mode**

The CPU fan activates when the power is turned on. It can be turned off when the CPU is in sleep mode. When in sleep mode, the CPU will not run at full power, thereby generating less heat.

## **CPU Overheat LED and Control**

This feature is available when the user enables the CPU overheat warning function in the BIOS. This allows the user to define an overheat temperature. When this temperature is exceeded, both the overheat fan and the warning LED are triggered.

## **System Resource Alert**

This feature is available when used with Intel's LANDesk Client Manager (optional). It is used to notify the user of certain system events. For example, if the system is running low on virtual memory and there is insufficient hard drive space for saving the data, you can be alerted of the potential problem.

## **Hardware BIOS Virus Protection**

The system BIOS is protected by hardware that prevents viruses from infecting the BIOS area. The user can only change the BIOS content through the flash utility provided by SUPERMICRO. This feature can prevent viruses from infecting the BIOS area and destroying valuable data.

## **Auto-Switching Voltage Regulator for the CPU Core**

The auto-switching voltage regulator for the CPU core can support up to 20A current and auto-sense voltage IDs ranging from 1.4V to 3.5V. This will allow the regulator to run cooler and thus make the system more stable.

## **1-5 ACPI/PC 98 Features**

ACPI stands for Advanced Configuration and Power Interface. The ACPI specification defines a flexible and abstract hardware interface that provides a standard way to integrate power management features throughout a PC system, including its hardware, operating system and application software. This enables the system to automatically turn on and off peripherals such as CD-ROMs, network cards, hard disk drives and printers. This also includes consumer devices connected to the PC such as VCRs, TVs, telephones and stereos.

In addition to enabling operating system-directed power management, ACPI provides a generic system event mechanism for Plug and Play and an operating system-independent interface for configuration control. ACPI lever-

ages the Plug and Play BIOS data structures while providing a processor architecture-independent implementation that is compatible with both Windows 98 and Windows NT 5.0.

**Note:** To utilize ACPI, you must reinstall Windows 98. To reinstall Windows 98 with ACPI, enter DOS and type "setup /p J" at the CDROM prompt (usually D:) with the Windows 98 CD loaded. (Make sure you include the spaces after "setup" and "p".) Then hit <Enter>. You can check to see if ACPI has been properly installed by looking for it in the Device Manager, which is located in the Control Panel in Windows.

### **Microsoft OnNow**

The OnNow design initiative is a comprehensive, system-wide approach to system and device power control. OnNow is a term for a PC that is always on but appears to be off and responds immediately to user or other requests.

### **Slow Blinking LED for Suspend-State Indicator**

When the CPU goes into a suspend state, the chassis power LED will start blinking to indicate that the CPU is in suspend mode. When the user presses any key, the CPU will wake-up and the LED will automatically stop blinking and remain on.

### **Main Switch Override Mechanism**

When an ATX power supply is used, the power button can function as a system suspend button to make the system enter a SoftOff state. The monitor will be suspended and the hard drive will spin down. Depressing the power button again will cause the whole system to wake-up. During the SoftOff state, the ATX power supply provides power to keep the required circuitry in the system alive. In case the system malfunctions and you want to turn off the power, just depress and hold the power button for 4 seconds. This option can be set in the Power section of the BIOS Setup routine.

### **External Modem Ring-On**

Wake-up events can be triggered by a device such as the external modem ringing when the system is in the SoftOff state. Note that external modem ring-on can only be used with an ATX 2.01 (or above) compliant power supply.

## Wake-On-LAN (WOL)

Wake-On-LAN is defined as the ability of a management application to remotely power up a computer that is powered off. Remote PC setup, updates and asset tracking can occur after hours and on weekends so that daily LAN traffic is kept to a minimum and users are not interrupted. The motherboards have a 3-pin header (WOL) to connect to the 3-pin header on a Network Interface Card (NIC) that has WOL capability. Wake-On-LAN must be enabled in BIOS. Note that Wake-On-Lan can only be used with an ATX 2.01 (or above) compliant power supply.

## 1-6 Power Supply

As with all computer products, a stable power source is necessary for proper and reliable operation. It is even more important for processors that have high CPU clock rates.

The SUPER P3TDE6/P3TDER accommodate ATX power supplies. Although most power supplies generally meet the specifications required by the CPU, some are inadequate. You should use one that will supply at least 300W of power - an even higher wattage power supply is recommended for high-load configurations. Also your power supply must provide a +5V standby voltage that supplies at least 720 mA of current. Also, for the P3TDE6, 1.5A is needed for LAN1 and LAN2.

It is strongly recommended that you use a high quality power supply that meets ATX power supply Specification 2.02 or above. Additionally, in areas where noisy power transmission is present, you may choose to install a line filter to shield the computer from noise. It is recommended that you also install a power surge protector to help avoid problems caused by power surges.

## 1-7 Super I/O

The disk drive adapter functions of the Super I/O chip include a floppy disk drive controller that is compatible with industry standard 82077/765, a data separator, write pre-compensation circuitry, decode logic, data rate selection, a clock generator, drive interface control logic and interrupt and DMA logic. The wide range of functions integrated onto the Super I/O greatly reduces the number of components required for interfacing with floppy disk drives. The Super I/O supports 360 K, 720 K, 1.2 M, 1.44 M or 2.88 M disk drives and data transfer rates of 250 Kb/s, 500 Kb/s or 1 Mb/s. It also

provides two high-speed, 16550 compatible serial communication ports (UARTs), one of which supports serial infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability and a processor interrupt system.

Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability and a processor interrupt system. Both UARTs provide legacy speed with baud rate of up to 115.2 Kbps as well as an advanced speed with baud rates of 250 K, 500 K, or 1 Mb/s, which support higher speed modems.

The Super I/O supports one PC-compatible printer port (SPP), Bi-directional Printer Port (BPP) , Enhanced Parallel Port (EPP) or Extended Capabilities Port (ECP).

The Super I/O provides functions that comply with ACPI (Advanced Configuration and Power Interface), which includes support of legacy and ACPI power management through an SMI or SCI function pin. It also features auto power management to reduce power consumption.

The IRQs, DMAs and I/O space resources of the Super I/O can flexibly adjust to meet ISA PnP requirements, which support ACPI and APM (Advanced Power Management).

## Chapter 2 Installation

### 2-1 Static-Sensitive Devices

Electric-Static-Discharge (ESD) can damage electronic components. To prevent damage to your system board, it is important to handle it very carefully. The following measures are generally sufficient to protect your equipment from ESD.

#### Precautions

- Use a grounded wrist strap designed to prevent static discharge.
- Touch a grounded metal object before removing the board from the anti-static bag.
- Handle the board by its edges only; do not touch its components, peripheral chips, memory modules or gold contacts.
- When handling chips or modules, avoid touching their pins.
- Put the motherboard and peripherals back into their antistatic bags when not in use.
- For grounding purposes, make sure your computer chassis provides excellent conductivity between the power supply, the case, the mounting fasteners and the motherboard.

#### Unpacking

The motherboard is shipped in antistatic packaging to avoid static damage. When unpacking the board, make sure the person handling it is static protected.

## 2-2 FCPGA Processor Installation



*When handling the FCPGA processor package, avoid placing direct pressure on the label area of the fan.*

This section covers the installation procedure for FCPGA (Flip Chip Plastic Grid Array) type processors. You should install the processor and heatsink first and then install the motherboard in the chassis. Following the installation procedures in the order they appear in this section should eliminate the most common problems encountered when installing a system.

**IMPORTANT:** Always connect the power cord last and always remove it before adding, removing or changing any hardware components.

### Processor

You are now ready to install the processors. Your P3TDE6/P3TDER motherboard has two 370-pin, FCPGA type sockets and can support single or dual Pentium® III 500 MHz-1.40 GHz FCPGA processors with a 512K L2 cache and single or dual low power Pentium® III processors (also with a 512K L2 cache) at front bus speeds of 133 and 100 MHz. Lift the lever on the FCPGA socket and install with the notched corner of the processor oriented with pin 1. Fully seat the processor into the socket and then close the lever. See Figure 2-1 for views of the FCPGA 370-pin socket before and after processor installation.

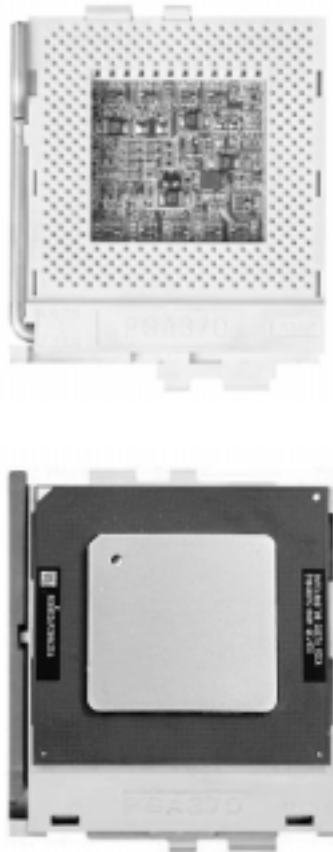
### Heatsink

Follow the instructions that came with your processor or heatsink to attach a heatsink to the processor. Your heatsink should have a 3-pin fan, which connects to the CPU FAN header. Make sure that good contact is made between the CPU chip (the die) and the heatsink. Insufficient contact or improper types of heatsinks, thermal compound, and/or fans can cause the processor to overheat, which may crash the system. (You can check the CPU temperature readings in the "Peripheral Setup" Section of BIOS.)

## Mounting the Motherboard in the Chassis

All motherboards have standard mounting holes to fit different types of chassis. Make sure the location of all the mounting holes for both the motherboard and the chassis match. Although a chassis may have both plastic and metal mounting fasteners, metal ones are highly recommended because they ground the motherboard to the chassis. Make sure the metal standoffs click in or are screwed in tightly. Then use a screwdriver to secure the motherboard onto the motherboard tray.

**Figure 2-1. FCPGA Socket: Empty and with Processor Installed (low power Pentium III shown)**



## 2-3 Installing DIMMs

**Note:** Check the Supermicro web site for recommended memory modules:  
[http://www.supermicro.com/TECHSUPPORT/FAQs/Memory\\_vendors.htm](http://www.supermicro.com/TECHSUPPORT/FAQs/Memory_vendors.htm)

---

### **CAUTION**

Exercise extreme care when installing or removing DIMM modules to prevent any possible damage. Also note that the memory is interleaved to improve performance (see step 1).

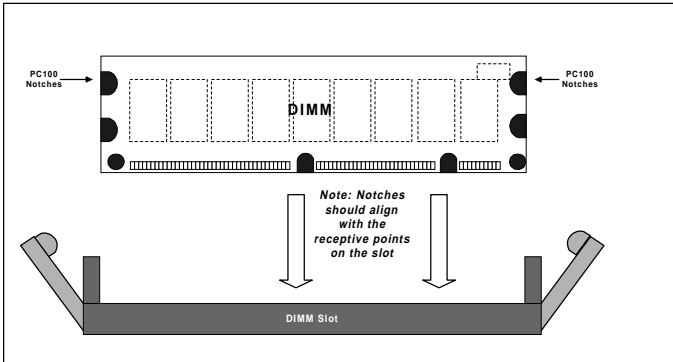
---

### **DIMM Installation (See Figure 2-2)**

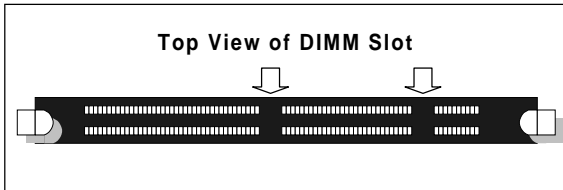
1. Insert either two or four DIMMs as required for the desired system memory. Two-way interleaved memory requires that memory modules be installed in pairs (first in the two slots of Bank0 and then in both slots of Bank1, if needed).
2. Insert each DIMM module vertically into its slot. Pay attention to the two notches along the bottom of the module to prevent inserting the DIMM module incorrectly.
3. Gently press down on the DIMM module until it snaps into place in the slot. Repeat for all modules (see step 1 above).

### **Support**

The P3TDE6/P3TDER only supports ECC registered SDRAM memory. PC133 and PC100 memory are both supported at their respective speeds. However, the memory bus is synchronized to the front side bus speed, so using PC100 with a 133 MHz FSB or using PC133 with a 100 MHz FSB, will result in 100 MHz memory speed operation in either case.

**Figure 2-2. Side View of DIMM Installation into Slot**

**To Install:** Insert module vertically and press down until it snaps into place. Pay attention to the notches.

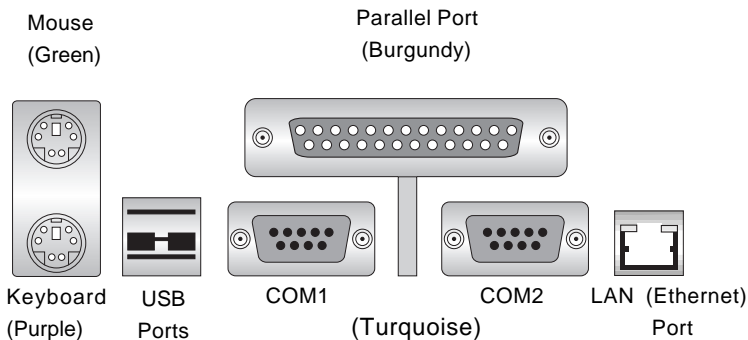


**To Remove:**

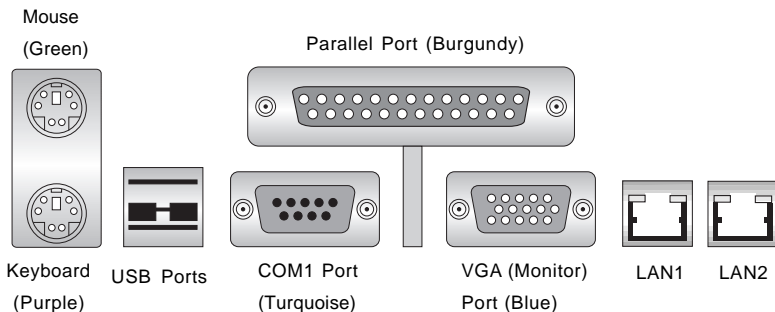
Use your thumbs to gently push near the edge of both ends of the module. This should release it from the slot.

## 2-4 I/O Ports/Control Panel Connectors

The I/O ports are color coded in conformance with the PC 99 specification. See Figure 2-3 below for the colors and locations of the various I/O ports.



**Figure 2-3a. I/O Port Locations and Definitions: P3TDE6**



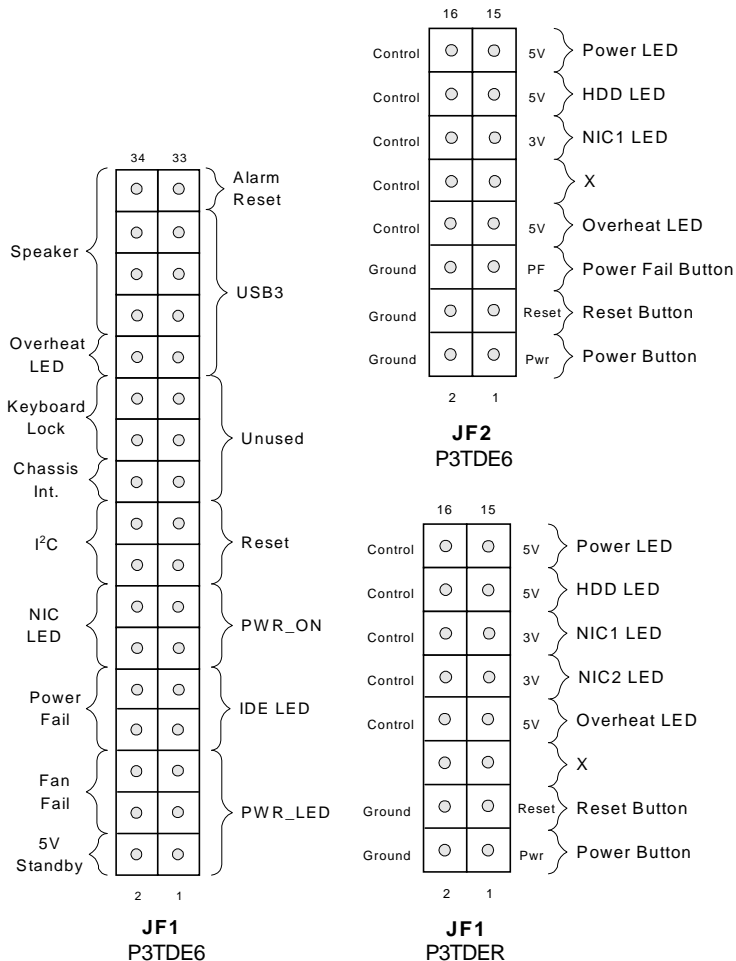
**Figure 2-3b. I/O Port Locations and Definitions: P3TDER**

**Note:** On the P3TDER, the COM2 connector is replaced by a VGA connector. COM2 is a header located near the Ultra160 SCSI channel B header (JA3) on the motherboard.

## Front Control Panel

JF1 on the P3TDE6 and JF2 on the P3TDE6 contain header pins for various front control panel connectors. These connectors are designed for use with Supermicro server chassis. JF1 on the P3TDE6 contains many of these same connections. It is provided for use with other chassis. See Figure 2-4 for the pin locations of the various front control panel buttons and LED indicators. Refer to the following section for descriptions and P3TDE6 JF1 pin definitions.

**Figure 2-4. JF1/JF2 Header Pins**



## 2-5 Connecting Cables

### Power Supply Connector

#### P3TDE6 20-pin connector:

After you have installed the motherboard, memory and PCI cards, you are ready to connect the cables. For the P3TDE6, attach an ATX power supply cable to either ATX#1 or ATX#2. PWR\_SEC is used only when you have dual CPUs. See the table on the right for pin definitions.

**ATX Power Supply 20-pin Connector  
Pin Definitions (P3TDE6)**

Pin Number	Definition	Pin Number	Definition
1	3.3V	11	3.3V
2	3.3V3	12	-12V
3	Ground	13	Ground
4	5V	14	PS-ON
5	Ground	15	Ground
6	5V	16	Ground
7	Ground	17	Ground
8	PW-OK	18	-5V
9	5VSB	19	5V
10	12V	20	5V

#### P3TDER 24-pin connector:

The power supply connector on the P3TDER meets the SSI (Superset ATX) 24-pin specification, however it also supports a 20-pin PS connector. Make sure that the orientation of the PS connector is correct. See the table on the right for pin definitions.

**ATX Power Supply 24-pin Connector  
Pin Definitions (P3TDER)**

Pin Number	Definition	Pin Number	Definition
13	+3.3V	1	+3.3V
14	-12V	2	+3.3V
15	COM	3	COM
16	PS_ON#	4	+5V
17	COM	5	COM
18	COM	6	+5V
19	COM	7	COM
20	Res(NC)	8	PWR_OK
21	+5V	9	5VSB
22	+5V	10	+12V
23	+5V	11	+12V
24	COM	12	+3.3V

### Power LED

The Power LED connection is located on JF1/JF2. Refer to the table on the right for P3TDE6 JF1 or page 2-7 for JF1/JF2 pin definitions.

**PWR\_LED Pin Definitions  
(JF1)**

Pin Number	Definition
1	+5V
3	Key
5	GND

### IDE/HDD LED

The IDE/HDD (Hard Drive) LED connection is located on JF1/JF2. Attach the IDE hard drive LED cable to the correct pins to display disk activity. Refer to the table on the right for P3TDE6 JF1 or page 2-7 for JF1/JF2 pin definitions.

**IDE\_LED Pin  
Definitions  
(JF1)**

Pin Number	Definition
7	+5V
9	HD Active

## PWR\_ON

The PWR\_ON connection is located on JF1/JF2. Momentarily contacting both pins will power on/off the system. This button can also be configured to function as a suspend button (see the Power Button Mode setting in BIOS). To turn off the power when set to suspend mode, depress the button for at least 4 seconds. Refer to the table on the right for P3TDE6 JF1 or page 2-7 for JF1/JF2 pin definitions.

**PWR\_ON Connector  
Pin Definitions  
(JF1)**

Pin Number	Definition
11	PW_ON
13	Ground

## NIC\_LED

The Network Interface Controller LED connection is located on JF1/JF2. Attach an NIC LED cable to display network activity. Refer to the table on the right for P3TDE6 JF1 or page 2-7 for JF1/JF2 pin definitions. **Note:** the P3TDER has two LAN ports and therefore connections for two NIC LEDs on JF1.

**NIC\_LED Pin  
Definitions  
(JF1)**

Pin Number	Definition
12	+5V
14	GND

## Reset

The Reset connection is located on JF1/JF2. Attach it to the hardware reset switch on the computer case. Refer to the table on the right for P3TDE6 JF1 or page 2-7 for JF1/JF2 pin definitions.

**Reset Pin  
Definitions  
(JF1)**

Pin Number	Definition
15	Reset
17	Ground

## I<sup>2</sup>C (P3TDE6 only)

The I<sup>2</sup>C connection is located on pins 16 and 18 of JF1. Refer to the table on the right for P3TDE6 JF1 or page 2-7 for JF1/JF2 pin definitions.

**I<sup>2</sup>C Pin Definitions  
(JF1)**

Pin Number	Definition
16	SDA
18	SCL

## Chassis Intrusion

A Chassis Intrusion connection is located on pin 20 of JF1 for the P3TDE6 and on JP52. See the tables on the right for pin definitions.

**Chassis Intrusion  
Pin Definitions (JF1)**

Pin Number	Definition
20	Intrusion Input

**Chassis Intrusion  
Pin Definitions (JP52)**

Pin Number	Definition
1	Signal
2	Ground

## Keyboard Lock (P3TDE6 only)

The Keyboard Lock connection is located on pins 22 and 24 of JF1 on the P3TDE6. See the table on the right for pin definitions.

**Keyboard Lock  
Pin Definitions  
(JF1)**

Pin Number	Definition
22	+5V
24	GND

## Overheat LED (OH)

Connect an LED to the OH connection on JF1/JF2 to provide advanced warning of chassis overheating. Refer to the table on the right for P3TDE6 JF1 or page 2-7 for JF1/JF2 pin definitions.

**Overheat LED (OH)  
Pin Definitions (JF1)**

Pin #	Definition
26	OH Active
25	PWR: Individual Connector only

## Extra Universal Serial Bus Connection (USB3)

An additional connection for USB3 is included on pins 25, 27, 29 and 31 of JF1 on the P3TDE6 and at J214 on the P3TDER for front side USB access. You will need a USB cable (not included) to use this connection.

**Note:** The USB4 (J105) connector is described on page 2-12.

**USB3 Pin  
Definitions (JF1)**

Pin Number	Definition
25	Power
27	-
29	+
31	Ground

**USB3 Pin  
Definitions (J214)**

Pin Number	Definition
1	+5V
2	Key
3	IRRX
4	Ground

## Speaker (P3TDE6 only)

The speaker connection is located on pins 28, 30, 32 and 34 of JF1 on the P3TDE6. See the table on the right for pin definitions.

**Speaker Connector Pin Definitions (JF1)**

Pin Number	Function	Definition
28	+ Key	Red wire, Speaker data
30		No connection
32		Key
34		Speaker data

## Fan Headers\*

The motherboard has CPU, chassis and overheat fan headers designated CPU, CHASSIS and OH FAN, respectively. See the table on the right for pin definitions.

**Fan Header Pin Definitions (CPU/CHASSIS/OH Fans)**

Pin Number	Definition
1	Ground (black)
2	+12V (red)
3	Tachometer

Caution: These fan headers are DC power.

## Serial Ports

On the P3TDE6, the COM1 and COM2 serial ports are located under the parallel port (see Figure 2-3). See the table on the right for pin definitions. On the P3TDER, the COM2 connector is a header located near the Ultra160 SCSI channel B header (JA3) on the motherboard.

**Serial Port Pin Definitions (COM1, COM2)**

Pin Number	Definition	Pin Number	Definition
1	DCD	6	CTS
2	DSR	7	DTR
3	Serial In	8	RI
4	RTS	9	Ground
5	Serial Out	10	NC

## ATX PS/2 Keyboard and PS/2 Mouse Ports

The ATX PS/2 keyboard and the PS/2 mouse are located on J18. See the table on the right for pin definitions. (The mouse port is above the keyboard port. See Figure 2-3.)

**PS/2 Keyboard and Mouse Port Pin Definitions (J18)**

Pin Number	Definition
1	Data
2	NC
3	Ground
4	VCC
5	Clock
6	NC

## Universal Serial Bus (USB)

Two Universal Serial Bus ports are located beside the keyboard/mouse ports. USB0 is the bottom connector and USB1 is the top connector. See the table on the right for pin definitions.

Universal Serial Bus Pin Definitions  
USB0                      USB1

Pin Number	Definition	Pin Number	Definition
1	+5V	1	+5V
2	P0-	2	P0-
3	P0+	3	P0+
4	Ground	4	Ground
5	N/A	5	Key

## Wake-On-LAN

The Wake-On-LAN header is designated as WOL. See the table on the right for pin definitions. You must enable the LAN Wake-Up setting in BIOS to use this feature. You must also have a LAN card with a Wake-on-LAN connector and cable.

Wake-On-LAN Pin Definitions (WOL)

Pin Number	Definition
1	+5V Standby
2	Ground
3	Wake-up

## Power Supply Fail Header (P3TDE6 only)

Connect a cable from your power supply to the header labelled JP54 to provide warning of power supply failure. This warning signal is passed through the PWR\_LED pin on JF1 to provide indication of a power failure on the chassis. This feature is only available when using Supermicro power supplies. See the table on the right for pin definitions.

Power Supply Fail Header Pin Definitions (JP54)

Pin Number	Definition
1	P/S 1 Fail Signal
2	P/S 2 Fail Signal
3	P/S 3 Fail Signal
4	Reset (from MB)

## SLED1 (SCSI LED) Indicator

The SLED connector is used to provide an LED indication of SCSI activity. See the table on the right for pin definitions.

SCSI LED Pin Definitions (SLED1)

Pin Number	Definition
1	Positive
2	Negative
3	Negative
4	Positive

## IPMB (P3TDER only)

An IPMB (Intelligent Platform Management Bus) connection is located at JP70. Connect the appropriate cable here to utilize IPMI on your system.

## SMB (P3TDER only)

An SMB (System Management Bus) connection is located at JP71. Connect the appropriate cable here to utilize SMB on your system.

## 2-6 DIP Switch Settings

### DIP Switch 1: Processor Speed

The red "DIP" switch labeled SW1 has four individual switches, which are used to set the speed of the processor (CPU).

The table on the right shows the switch settings for the various speeds your processor may be able to run at. The speeds on the left are for 100 MHz and those on the right are for 133 MHz front side bus speeds.

**Note:** Most Intel processors have a fixed speed that overwrites the setting of DIP Switch 1.

Processor Speed Selection  
(DIP Switch1)

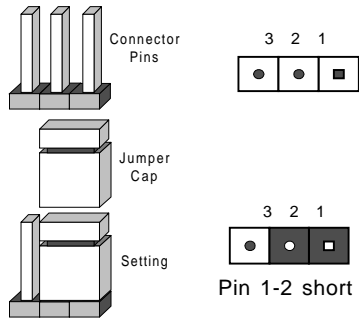
CPU Speed	SW #4	SW #3	SW #2	SW #1
500/666	ON			ON
550/733	ON			
600/800		ON	ON	ON
650/866		ON	ON	
700/933		ON		ON
750/1.0		ON		
800/1.064			ON	ON
850/1.13	ON	ON		ON
900/1.2	ON	ON		
950/1.26	ON	ON	ON	
1.0/1.33			ON	
1.05/1.4	ON		ON	ON

## 2-7 Jumper Settings

### Explanation of Jumpers

To modify the operation of the motherboard, jumpers can be used to choose between optional settings. Jumpers create shorts between two pins to change the function of the connector. Pin 1 is identified with a square solder pad on the printed circuit board. See the motherboard layout pages for jumper locations.

**Note:** On two pin jumpers, "Closed" means the jumper is on and "Open" means the jumper is off the pins.



### CMOS Clear

Refer to the table on the right for the jumper settings to clear CMOS. Always remove the AC power cord from the system before clearing CMOS. **NOTE:** For an ATX power supply, you must completely shut down the system, remove the AC power cord and *then* use JBT1 to clear CMOS. Replace JBT1 back to the pin 1-2 position before powering up the system again. Do not use the PW\_ON connector to clear CMOS.

**CMOS Clear Jumper Settings (JBT1)**

Jumper Position	Definition
1-2	Normal
2-3	CMOS Clear

Position 1-2

Normal

Position 2-3

CMOS Clear

## Front Side Bus Speed

CPU speed = FSB x Core/Bus ratio

Jumper JP1 allows you to set the FSB (Front Side Bus). See the table on the right for jumper settings.

See Section 2-6 for processor speed settings (DIP switch 1).

**Front Side (System) Bus Speed  
Jumper Settings (JP1)**

Jumper Position	Definition
1-2	Auto
2-3	100 MHz
OFF	133 MHz

Note: The Auto setting allows the CPU to set the speed.

## SCSI Termination Enable/ Disable

P3TDE6: Jumper JP60.

P3TDER: Jumper JP64.

The SCSI Termination jumper allows you to enable or disable termination for the SCSI connectors. The normal (default) position is open to enable SCSI termination. See the table on the right for jumper settings.

**SCSI Termination  
Enable/Disable  
Jumper Settings  
(JP60, JP64)**

Jumper Position	Definition
Open	Enabled
Closed	Disabled

## Watchdog Enable/Disable

JP64 (P3TDE6) and JP73 (P3TDER) allow you to enable or disable the Watchdog feature. The normal (default) position is open to disable the Watchdog timer and enable the speaker. This jumper setting works in conjunction with the setting in BIOS. See the table on the right for jumper settings.

**Watchdog  
Enable/Disable  
Jumper Settings  
(JP64, JP73)**

Jumper Position	Definition
Open	Disabled
Closed	Enabled

## SpeakerEnable/Disable

You may want to disable the onboard speaker. Jumper JP56 gives you this option. See the table on the right for jumper settings.

**Speaker Enable/Disable  
Jumper Settings (JP56)**

Jumper Position	Definition
Open	Disabled
Closed	Enabled

## Onboard LAN/NIC Enable/Disable

P3TDE6: Jumper JP58 only

P3TDER: Jumpers JP58 & JP62

Change the setting of jumper JP58/JP62 to enable or disable the onboard LAN or NIC (Network Interface Card) on the motherboard. See the table on the right for jumper settings. The default setting is open.

**Onboard LAN1/LAN2  
Enable/Disable  
Jumper Settings  
(JP58 & JP62)**

Jumper Position	Definition
Open	Enabled
Closed	Disabled

## Third Power Supply Failure Alarm Enable/Disable (P3TDE6 only)

This feature is for Supermicro Hot-Swap Triple Redundant Power Supplies only. When enabled, the system will notify you in the event of a power supply failure. This feature assumes that three power supply units are installed in the chassis, with one acting as a backup. If you only have one or two power supply units installed, you should disable this with JP55 to prevent false alarms. See the table on the right for jumper settings.

**Power Supply Failure  
Alarm Enable/Disable  
Jumper Settings (JP55)**

Jumper Position	Definition
Open	Disabled
Closed	Enabled

## LVD Channel A SCSI Termination Enable/Disable

Jumper JA2 allows you to enable or disable termination for the LVD Channel A SCSI connector. The normal (default) position is open to enable SCSI termination. See the table on the right for jumper settings.

**LVD CH A SCSI  
Termination  
Jumper Settings (JA2)**

Jumper Position	Definition
Open	Enabled
Closed	Disabled

## LVD Channel B SCSI Termination Enable/Disable

Jumper JA4 allows you to enable or disable termination for the LVD Channel B SCSI connector. The normal (default) position is open to enable SCSI termination. See the table on the right for jumper settings.

**LVD CH B SCSI  
Termination  
Jumper Settings (JA4)**

Jumper Position	Definition
Open	Enabled
Closed	Disabled

## Ultra (50-pin) Channel B SCSI Termination Enable/Disable (P3TDE6 only)

Jumper JA6 allows you to enable or disable termination for the 50-pin Ultra SCSI Channel B connector. The normal (default) position is open to enable SCSI termination. See the table on the right for jumper settings.

**50-pin Ultra SCSI CH B  
Termination  
Jumper Settings (JA6)**

Jumper Position	Definition
Open	Enabled
Closed	Disabled

## Spread Spectrum Enable/Disable

Jumper JP3 is used to enable or disable the Spread Spectrum feature. Spread Spectrum is a technique used to stabilize operation when a system is being affected by electromagnetic interference. The normal (default) position is open to disable Spread Spectrum. See the table on the right for jumper settings.

**Spread Spectrum  
Jumper Settings (JP3)**

Jumper Position	Definition
Open	Disabled
Closed	Enabled

## BIOS Select (P3TDE6 only)

Jumper JP57 allows you to select either BIOS chip 1 or BIOS chip 2 to boot the system with. The default position is on pins 1 and 2 to select BIOS 1. See the table on the right for jumper settings.

**BIOS Select  
Jumper Settings (JP57)**

Jumper Position	Definition
1-2	BIOS 1
2-3	BIOS 2

## PCI 66/33 MHz Select (P3TDE6 only)

Jumper JP61 allows you to set the two 3V PCI-64 slots on the P3TDE6 to run at either 66 or 33 MHz. The default position is open to enable 66 MHz operation. See the table on the right for jumper settings.

**PCI 66/33 MHz Select  
Jumper Settings (JP61)**

Jumper Position	Definition
Open	66 MHz
Closed	33 MHz

## Thermal Fan Enable/Disable

JP62 (P3TDE6) and JP65 (P3TDER) allow you to enable or disable continuous operation of the thermal fan. The default position is open to disable operation. See the table on the right for jumper settings.

**Thermal Fan Enable/  
Disable Jumper Settings  
(JP62, JP65)**

Jumper Position	Definition
Open	Disabled
Closed	Enabled

## CPU/CPU Chassis Fan Select

JP65 (P3TDE6) and JP72 (P3TDER) allow you to select to use either the CPU fan or the CPU Chassis fan. The default position is closed to select the CPU fan. See the table on the right for jumper settings.

**CPU/CPU Chassis Fan  
Select Jumper Settings  
(JP65, JP72)**

Jumper Position	Definition
Open	CPU Chassis
Closed	CPU

## VGA Enable/Disable (P3TDER only)

JP68 allows you to enable or disable the VGA port. The default position is on pins 1 and 2 to enable VGA. See the table on the right for jumper settings.

**VGA Enable/Disable  
Jumper Settings  
(JP68)**

Jumper Position	Definition
1-2	Enabled
2-3	Disabled

## 2-8 Parallel Port, Floppy/Hard Disk Drive and SCSI Connections

Note the following when connecting the floppy and hard disk drive cables:

- The floppy disk drive cable has seven twisted wires.
- A red mark on a wire typically designates the location of pin 1.
- A single floppy disk drive ribbon cable has 34 wires and two connectors to provide for two floppy disk drives. The connector with twisted wires always connects to drive A, and the connector that does not have twisted wires always connects to drive B.

### Parallel Port Connector

The parallel port is located on J16. See the table on the right for pin definitions.

**Parallel (Printer) Port Pin Definitions  
(J16)**

Pin Number	Function	Pin Number	Function
1	Strobe-	2	Auto Feed-
3	Data Bit 0	4	Error-
5	Data Bit 1	6	Init-
7	Data Bit 2	8	SLCT IN-
9	Data Bit 3	10	GND
11	Data Bit 4	12	GND
13	Data Bit 5	14	GND
15	Data Bit 6	16	GND
17	Data Bit 7	18	GND
19	ACK	20	GND
21	BUSY	22	GND
23	PE	24	GND
25	SLCT	26	NC

## Floppy Connector

The floppy connector is located on J15. See the table on the right for pin definitions.

**Floppy Connector Pin Definitions (JP15)**

Pin Number	Function	Pin Number	Function
1	GND	2	FDHDIN
3	GND	4	Reserved
5	Key	6	FDEDIN
7	GND	8	Index-
9	GND	10	Motor Enable
11	GND	12	Drive Select B-
13	GND	14	Drive Select A-
15	GND	16	Motor Enable
17	GND	18	DIR-
19	GND	20	STEP-
21	GND	22	Write Data-
23	GND	24	Write Gate-
25	GND	26	Track 00-
27	GND	28	Write Protect-
29	GND	30	Read Data-
31	GND	32	Side 1 Select-
33	GND	34	Diskette

## IDE Connectors

There are no jumpers to configure the onboard IDE connectors J13 and J14. See the table on the right for pin definitions.

**IDE Connector Pin Definitions  
(J13, J14)**

Pin Number	Function	Pin Number	Function
1	Reset IDE	2	GND
3	Host Data 7	4	Host Data 8
5	Host Data 6	6	Host Data 9
7	Host Data 5	8	Host Data 10
9	Host Data 4	10	Host Data 11
11	Host Data 3	12	Host Data 12
13	Host Data 2	14	Host Data 13
15	Host Data 1	16	Host Data 14
17	Host Data 0	18	Host Data 15
19	GND	20	Key
21	DRQ3	22	GND
23	I/O Write-	24	GND
25	I/O Read-	26	GND
27	IOCHRDY	28	BALE
29	DACK3-	30	GND
31	IRQ14	32	IOCS16-
33	Addr 1	34	GND
35	Addr 0	36	Addr 2
37	Chip Select 0	38	Chip Select 1-
39	Activity	40	GND

## Ultra160 SCSI Connector

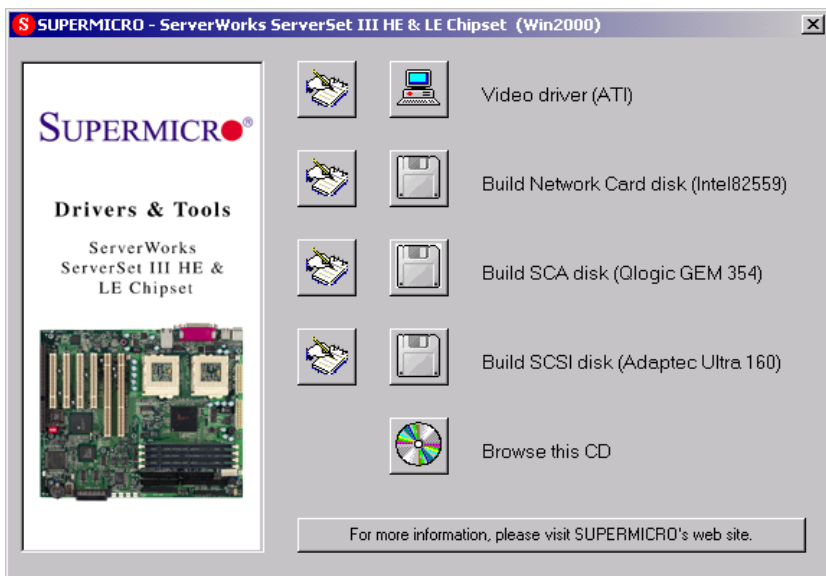
Refer to the table below for the pin definitions of the Ultra160 SCSI connectors located at JA1, JA3 and JA5.

68-pin Ultra160 SCSI Connectors (JA1, JA3, JA5)

Connector Contact Number	Signal Names	Connector Contact Number	Signal Names
1	+DB(12)	35	-DB(12)
2	+DB(13)	36	-DB(13)
3	+DB(14)	37	-DB(14)
4	+DB(15)	38	-DB(15)
5	+DB(P1)	39	-DB(P1)
6	+DB(0)	40	-DB(0)
7	+DB(1)	41	-DB(1)
8	+DB(2)	42	-DB(2)
9	+DB(3)	43	-DB(3)
10	+DB(4)	44	-DB(4)
11	+DB(5)	45	-DB(5)
12	+DB(6)	46	-DB(6)
13	+DB(7)	47	-DB(7)
14	+DB(P)	48	-DB(P)
15	GROUND	49	GROUND
16	DIFFSENS	50	GROUND
17	TERMPWR	51	TERMPWR
18	TERMPWR	52	TERMPWR
19	RESERVED	53	RESERVED
20	GROUND	54	GROUND
21	+ATN	55	-ATN
22	GROUND	56	GROUND
23	+BSY	57	-BSY
24	+ACK	58	-ACK
25	+RST	59	-RST
26	+MSG	60	-MSG
27	+SEL	61	-SEL
28	+C/D	62	-C/D
29	+REQ	63	-REQ
30	+I/O	64	-I/O
31	+DB(8)	65	-DB(8)
32	+DB(9)	66	-DB(9)
33	+DB(10)	67	-DB(10)
34	+DB(11)	68	-DB(11)

## 2-9 Installing Software Drivers

After all the hardware has been installed you must install the software drivers. The necessary drivers are all included on the Supermicro CD that came packaged with your motherboard. After inserting this CD into your CDROM drive, the display shown in Figure 2-5 should appear. (If this display does not appear, click on the My Computer icon and then on the icon representing your CDROM drive. Finally, double click on the S "Setup" icon.)



**Figure 2-5. Driver/Tool Installation Display Screen**

Click the icons showing a hand writing on paper to view the readme files for each item. The bottom icon with a CD on it allows you to view the entire contents of the CD.

Build SCA disk (QLogic GEM 354): For integration with the SuperServer SC850 and SC860 chassis.

## Chapter 3

# Troubleshooting

### 3-1 Troubleshooting Procedures

Use the following procedures to troubleshoot your system. If you have followed all of the procedures below and still need assistance, refer to the 'Technical Support Procedures' and/or 'Returning Merchandise for Service' section(s) in this chapter.

**Note: Always disconnect the power cord before adding, changing or installing any hardware components.**

#### Before Power On

1. Make sure no short circuits exist between the motherboard and chassis.
2. Disconnect all ribbon/wire cables from the motherboard, including those for the keyboard and mouse.
3. Remove all add-on cards.
4. Install one CPU (making sure it is fully seated) and connect the chassis speaker and the power LED to the motherboard. (Check all jumper settings as well.)

#### No Power

1. Make sure no short circuits exist between the motherboard and the chassis.
2. Verify that all jumpers are set to their default positions.
3. Check that the 115V/230V switch on the power supply is properly set.
4. Turn the power switch on and off to test the system.
5. The battery on your motherboard may be old. Check to verify that it still supplies ~3VDC. If it does not, replace it with a new one.

#### No Video

1. If the power is on but you have no video, remove all the add-on cards and cables.
2. Use the speaker to determine if any beep codes exist. Refer to Appendix A for details on beep codes.

---

### **NOTE**

If you are a system integrator, VAR or OEM, a POST diagnostics card is recommended. For I/O port 80h codes, refer to App. B.

---

## **Memory Errors**

1. Make sure the DIMM modules are properly and fully installed in pairs.
2. Determine if different speeds of DIMMs have been installed and verify that the BIOS setup is configured for the fastest speed of RAM used. It is recommended to use the same RAM speed for all DIMMs in the system.
3. Make sure you are using PC133 or PC100 compliant, registered ECC, SDRAM. EDO SDRAM is not supported.
4. Check for bad DIMM modules or slots by swapping a single module between two slots and noting the results.
5. Make sure all memory modules are fully seated in their slots.
6. Check the power supply voltage 115V/230V switch.

## **Losing the System's Setup Configuration**

1. Check the setting of jumper JBT1. Ensure that you are using a high quality power supply. A poor quality power supply may cause the system to lose the CMOS setup information. Refer to page 1-19 for details on recommended power supplies.
2. The battery on your motherboard may be old. Check to verify that it still supplies ~3VDC. If it does not, replace it with a new one.
3. If the above steps do not fix the Setup Configuration problem, contact your vendor for repairs.

## **3-2 Technical Support Procedures**

Before contacting Technical Support, please take the following steps. Also, note that as a motherboard manufacturer, Super Micro does not sell directly to end-users, so it is best to first check with your distributor or reseller for troubleshooting services. They should know of any possible problem(s) with the specific system configuration that was sold to you.

1. Please go through the 'Troubleshooting Procedures' and 'Frequently Asked Question' (FAQ) sections in this chapter or see the FAQs on our

web site (<http://www.supermicro.com/techsupport.htm>) before contacting Technical Support.

2. BIOS upgrades can be downloaded from our web site at <http://www.supermicro.com/techsupport/download.htm>.

**Note: Not all BIOS can be flashed depending on the modifications to the boot block code.**

3. If you still cannot resolve the problem, include the following information when contacting Super Micro for technical support:

- Motherboard model and PCB revision number
- BIOS release date/version (this can be seen on the initial display when your system first boots up)
- System configuration

An example of a Technical Support form is on our web site at [http://www.supermicro.com/techsupport/contact\\_support.htm](http://www.supermicro.com/techsupport/contact_support.htm).

4. Distributors: For immediate assistance, please have your account number ready when placing a call to our technical support department. We can be reached by e-mail at [support@supermicro.com](mailto:support@supermicro.com) or by fax at: (408) 503-8000, option 2.

### 3-3 Frequently Asked Questions

**Question: What are the various types of memory that the P3TDE6/P3TDER motherboard can support?**

**Answer:** The P3TDE6/P3TDER have four DIMM slots that support 168-pin, registered ECC DIMMs only. Unbuffered SDRAM or non-ECC memory is not supported. PC133 and PC100 memory are both fully supported at their respective speeds. **Important: The memory employs a two-way interleaving scheme, which requires you to install memory modules in pairs (first in the two slots of Bank0, and then, in both slots of Bank1, if needed.)**

**Question: How do I update my BIOS?**

**Answer:** It is recommended that you **do not** upgrade your BIOS if you are experiencing no problems with your system. Updated BIOS files are located on our web site at <http://www.supermicro.com>. Please check our BIOS warning message and the info on how to update your BIOS on our web site. Also, check the current BIOS revision and make sure it is newer than

your BIOS before downloading. Select your motherboard model and download the BIOS file to your computer. Unzip the BIOS update file and you will find the readme.txt (flash instructions), the flash.bat (BIOS flash utility) and the BIOS image (xxxxxx.rom) files. Copy these files onto a bootable floppy and reboot your system. It is not necessary to set BIOS boot block protection jumpers on the motherboard. At the DOS prompt, enter the command "flash." This will start the flash utility and give you an opportunity to save your current BIOS image. Flash the boot block and enter the name of the update BIOS image file.

**Note:** It is important to save your current BIOS and **rename it "super.rom"** in case you need to recover from a failed BIOS update. Select flash boot block, then enter the update BIOS image. Select "Y" to start the BIOS flash procedure and do not disturb your system until the flash utility displays that the procedure is complete. After updating your BIOS, please clear the CMOS then load Optimal Values in the BIOS.

**Question: After flashing the BIOS my system does not have video. How can I correct this?**

**Answer:** If the system does not have video after flashing your new BIOS, it indicates that the flashing procedure failed. To remedy this, first clear CMOS per the instructions in this manual and retry the BIOS flashing procedure. If you still do not have video, please use the following **BIOS Recovery Procedure**. First, make sure the JPWAKE jumper is disabled. Then, turn your system off and place the floppy disk with the saved BIOS image file (see above FAQ) in drive A. Press and hold <CTRL> and <Home> at the same time, then turn on the power with these keys pressed until your floppy drive starts reading. Your screen will remain blank until the BIOS program is done. If the system reboots correctly, then the recovery was successful. The BIOS Recovery Procedure will not update the boot block in your BIOS.

**Question: What's on the CD that came with my motherboard?**

**Answer:** The supplied compact disc has quite a few drivers and programs that will greatly enhance your system. We recommend that you review the CD and install the applications you need. Applications on the CD include chipset drivers for Windows and security and audio drivers.

**Question: Why can't I turn off the power using the momentary power on/off switch?**

**Answer:** The instant power off function is controlled in BIOS by the Power Button Mode setting. When the On/Off feature is enabled, the motherboard will have instant off capabilities as long as the BIOS has control of the system. When the Standby or Suspend feature is enabled or when the BIOS is not in control such as during memory count (the first screen that appears when the system is turned on), the momentary on/off switch must be held for more than four seconds to shut down the system. This feature is required to implement the ACPI features on the motherboard.

### **3-4 Returning Merchandise for Service**

A receipt or copy of your invoice marked with the date of purchase is required before any warranty service will be rendered. You can obtain service by calling your vendor for a Returned Merchandise Authorization (RMA) number. When returning to the manufacturer, the RMA number should be prominently displayed on the outside of the shipping carton, and mailed prepaid or hand-carried. Shipping and handling charges will be applied for all orders that must be mailed when service is complete.

This warranty only covers normal consumer use and does not cover damages incurred in shipping or from failure due to the alternation, misuse, abuse or improper maintenance of products.

During the warranty period, contact your distributor first for any product problems.

**Notes**

# Chapter 4

## BIOS

### 4-1 Introduction

This chapter describes the AMIBIOS for the P3TDE6/P3TDER. The AMI ROM BIOS is stored in a Flash EEPROM and can be easily upgraded using a floppy disk-based program.

**Note:** Due to periodic changes to BIOS, some settings may have been added or deleted and might not yet be recorded in this manual. Refer to the Manual Download area of our web site for any changes to BIOS that are not reflected in this manual.

#### System BIOS

The BIOS is the Basic Input Output System used in all IBM® PC, XT™, AT®, and PS/2® compatible computers. The BIOS ROM stores the system parameters, such as amount of memory, type of disk drives and video displays, etc. BIOS ROM requires very little power. When the computer is turned off, a back-up battery provides power to the BIOS ROM, enabling it to retain the system parameters. Each time the computer is powered-on, the computer is then configured with the values stored in the BIOS ROM by the system BIOS, which gains control when the computer is powered on.

#### How To Change the Configuration Data

The configuration data that determines the system parameters may be changed by entering the BIOS Setup utility. This Setup utility can be accessed by pressing <Del> at the appropriate time during system boot.

#### Starting the Setup Utility

Normally, the only visible POST (Power On Self Test) routine is the memory test. As the memory is being tested, press the <Delete> key to enter the main menu of the BIOS Setup utility. From the main menu, you can access the other setup screens, such as the Chipset and Power menus. Section 4-3 gives detailed descriptions of each parameter setting in the Setup utility.

An AMIBIOS identification string is displayed at the left bottom corner of the screen, below the copyright message.

## 4-2 BIOS Features

- Supports Plug and Play V1.0A and DMI 2.3
- Supports Intel PCI (Peripheral Component Interconnect) (PME) local bus specification 2.2
- Supports Advanced Power Management (APM) specification v 1.1
- Supports ACPI
- Supports Flash ROM

AMIBIOS supports the LS120 drive made by Matsushita-Kotobuki Electronics Industries Ltd. The LS120:

- Can be used as a boot device
- Is accessible as the next available floppy drive

AMIBIOS supports PC Health Monitoring chips. When a failure occurs in a monitored activity, AMIBIOS can sound an alarm and display a message. The PC Health Monitoring chips monitor:

- CPU temperature
- Chassis intrusion detector
- Five positive voltage inputs
- Four fan speed monitor inputs

## 4-3 Running Setup

*\*Optimal default settings are in bold text unless otherwise noted.*

The BIOS setup options described in this section are selected by choosing the appropriate text from the Standard Setup screen. All displayed text is described in this section, although the screen display is often all you need to understand how to set the options (see on next page).

## The Main BIOS Setup Menu

Press the <Delete> key during the POST (Power On Self Test) to enter the Main Menu of the BIOS Setup Utility. All Main Setup options are described in this section. The Main BIOS Setup screen is displayed below.

BIOS SETUP UTILITY	
<b>Main</b> Advanced Chipset PCIPnP Power Boot Security Exit	
AMIBIOS Version : 07.00xx BIOS Build Date : xx/xx/xx BIOS ID :  Processor Type : PentiumIII™ Processor Speed : 933MHz  System Memory : 256MB  System Time [10:10:00] System Date [Thu 08/24/00]	↔ Select Screen ↑↓ Select Item +- Change Field Tab Select Field F1 General Help F10 Save and Exit ESC Exit
V02.03 (C)Copyright 1985-2000, American Megatrends, Inc.	

Use the Up/Down arrow keys or the <Tab> key to move between the different settings in the above menu.

When the items "System Time", and "System Date" are highlighted, type in the correct time/date in the time field, and then press "Enter". The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format. The time is in also 24-hour format. For example, 5:30 a.m. appears as 05:30:00 and 5:30 p.m. as 17:30:00.

Press the <ESC> key to exit the Main Menu and use the Left/Right arrow keys to enter the the other categories of BIOS settings. The next section is described in detail to illustrate how to navigate through the menus.

**Note:** Items displayed in gray are preset and cannot be selected. Items with a blue arrow are commands, not options (i.e. Discard Changes).

## 4-4 Advanced BIOS Setup

Choose Advanced BIOS Setup from the AMIBIOS Setup Utility main menu with the Left/Right arrow keys. You should see the following display. Select one of the items in the left frame of the screen, such as SuperIO Configuration, to go to the sub screen for that item. Advanced BIOS Setup options are displayed by highlighting the option using the arrow keys. All Advanced BIOS Setup options are described in this section.

BIOS SETUP UTILITY	
Main	Advanced
Chipset    PCI/PnP    Power    Boot    Security    Exit  Setup Warning Setting items on this screen to incorrect values may cause the system to malfunction!  > SuperIO Configuration > IDE Configuration > Floppy Configuration > Boot Settings Configuration > Event Log Configuration > Peripheral Device Configuration > System Health Monitor > Remote Access Configuration	Configure SuperIO Chipset Winbond627F       ↔ Select Screen ↑↓ Select Item Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit
V7.00 (C)Copyright 1985-2001, American Megatrends, Inc.	

Use the Up/Down arrow keys to select the "Super I/O Configuration" line.

When the "Super IO Configuration" line is highlighted, hit "ENTER" to display its menu.

The following Super IO Configuration screen will appear. Here you can select your options for the your computer's I/O (Input/Output) devices.

## Super I/O Configuration

BIOS SETUP UTILITY	
Advanced	
Configure Winbond627F Serial Port(s) and Parallel P	
Serial Port1 Address	[3F8]
Serial Port1 IRQ	[4]
Serial Port2 Address	[2F8]
Serial Port2 IRQ	[3]
Serial Port2 Mode	[Normal]
Parallel Port Address	[378]
Parallel Port IRQ	[7]
Parallel Port Mode	[ECP]
ECP Mode DMA Channel	[3]
	↔ Select Screen ↑↓ Select Item +- Change Option F1 General Help F10 Save and Exit ESC Exit
V07.00 (C)Copyright 1985-2001, American Megatrends, Inc.	

The Super IO Configuration includes the following items:

### **Serial Port 1 Address**

This option specifies the base I/O port address of serial port 1. The settings for this item include Disabled, **3F8** and 3E8 and 2E8. Select the desired setting and then press "Enter".

### **Serial Port 1 IRQ**

This option specifies the Interrupt Request address of serial port 1. The settings for this item include Disabled, **4** and 3.

### **Serial Port 2 Address**

This option specifies the base I/O port address of serial port 2. The settings for this item include Disabled, **2F8**, 3E8 and 2E8.

### **Serial Port 2 IRQ**

This option specifies the Interrupt Request address of serial port 2. The settings for this item include Disabled, 4 and 3.

### **Serial Port 2 Mode**

You may use this setting when connecting an infrared device to serial port 2. The settings are **Normal**, Sharp-IR, SIR and Consumer.

### **Parallel Port Address**

This option specifies the I/O address used by the parallel port. The settings for this item include Disabled, **378**, 278 and 3BC. Select your setting and then press "Enter".

### **Parallel Port IRQ**

This option allows the user to set the Parallel Port IRQ. The settings for this item include 5 and 7.

### **Parallel Port Mode**

This option specifies the parallel port mode. The settings for this item include Normal, Bi-directional, EPP and **ECP**.

### **ECP Mode DMA Channel**

This option allows the user to set the setting for the ECP Mode of the DMA Channel. The settings for this item include **0**, 1 and 3.

## **IDE Configuration**

### **Primary IDE Master**

When entering "Setup", BIOS automatically detects the presence of IDE devices. This displays the auto detection status of the IDE devices. You can also manually configure the IDE drives by providing the following information:

This option allows the user to configure the IDE devices. When the desired item is highlighted (selected), press "Enter" and the following screen will be displayed:

#### **Type**

This option sets the type of device that the AMIBIOS attempts to boot from after AMIBIOS POST is completed. The settings include Not installed, **Auto**, CDROM and ARMD. The "Auto" setting allows BIOS to automatically detect the presence of the IDE controller.

#### **LBA/Large Mode**

LBA (Logical Block Addressing) is a method of addressing data on a disk drive. In LBA mode, the maximum drive capacity is 137 GB. The settings are Disabled and **Auto**. Select "Disabled" to disable LBA mode. Select "Auto" to enable LBA mode if your device supports it and is not already formatted with the LBA mode.

#### **Block (Multi-Sector Transfer) Mode**

This option sets the block mode multi sector transfers option. The settings include Disabled and **Auto**. Disabled: This option prevents the BIOS from using Multi-Sector Transfer on the specified channel. The data to and from the device will occur one sector at a time. Auto: This option allows the BIOS to auto detect device support for Multi-Sector Transfers on the specified channel. If supported, this option allows the BIOS to auto detect the number of sectors per block for transfer from the hard disk drive to memory. The data transfer to and from the device will occur multiple sectors at a time (if the device supports it).

### **PIO Mode**

IDE PIO (Programmable I/O) mode programs timing cycles between the IDE drive and the programmable IDE controller. As the PIO mode increases, the cycle time decreases. The settings are: **Auto**, 0, 1, 2, 3 and 4.

### **DMA Mode**

This item allows the users to select the DMA mode. The settings are: **Auto**, SWDMA0, SWDMA1, SWDMA2, MWDMA0, MWDMA1, MWDMA2, UWDMA0, UWDMA1, UWDMA2, UWDMA3 and UWDMA4. Select Auto to auto detect the DMA Mode. Select SWDMA0 through SWDMA2 to set single word DMA0 through DMA2. Select MWDMA0 through MWDMA2 to set Multi-word DMA0 through DMA2. Select UDMA0 through UDMA4 to set Ultra DMA0 through Ultra DMA4.

### **S.M.A.R.T.**

S.M.A.R.T stands for Self-Monitoring Analysis and Reporting Technology, a feature that can help predict impending drive failures. The settings are **Auto**, Disabled and Enabled. Select "Enabled" or "Disabled" to enable or disable the S.M.A.R.T. Select "Auto" to auto detect S.M.A.R.T.

### **32Bit Data Transfer**

The settings are Auto, Disabled and **Enabled**. Select "Enabled" or "Disabled" to enable or disable the 32-bit Data Transfer function. Select "Auto" to auto detect the 32-bit Data Transfer function.

### **ARMD Emulation Type**

This option is used to select the emulation used when configuring an LS120, MO (Magneto-Optical), or Iomega Zip drive. The settings are **Auto**, Floppy and HardDisk.

### **Primary IDE Slave**

When the system enters "Setup", BIOS automatically detects the presence of IDE devices. This option displays the auto detection status of IDE devices. The settings for "Primary IDE Slave" are the same as those for the "Primary IDE Master".

### **Secondary IDE Master**

This displays the status of auto detection of IDE devices. The settings for "Secondary IDE Master" are the same as those for the "Primary IDE Master".

### **Secondary IDE Slave**

This displays the status of auto detection of IDE devices. The settings for "Secondary IDE Slave" are the same as those for the "Primary IDE Master".

### **Hard Disk Write Protect**

This item allows the user to prevent the hard disk from being overwritten. The options are Enabled or **Disabled**. Enabled allows the drive to be used normally; read, write and erase functions can all be performed. Disabled prevents the hard disk from being erased. This function is effective only when the device is accessed through BIOS.

## **Floppy Configuration**

### **Floppy A**

Use this option to specify which of floppy drive you have installed in the A drive. The settings are Disabled, 360 KB 5 1/4", 1.2 MB 5 1/4", 720 KB 3 1/2", **1.44 MB 3 1/2"** and 2.88 MB 3 1/2".

### **Floppy B**

Use this option to specify which of floppy drive you have installed in the B drive. The settings are Disabled, 360 KB 5 1/4", 1.2 MB 5 1/4", 720 KB 3 1/2", **1.44 MB 3 1/2"** and 2.88 MB 3 1/2".

### **Floppy Drive Seek**

Use this option to Enable or **Disable** the floppy seek routine on bootup.

## **Boot Settings Configuration**

### **Quick Boot**

This option allows the BIOS to skip certain tests that are normally performed on boot up. You can disable the option to speed up boot time. The settings are **Disabled** and Enabled.

### **Quiet Boot**

If Disabled, this option will cause the normal POST messages to be displayed upon setup. When Enabled, the OEM logo is displayed instead of the POST messages. The settings are Enabled, and **Disabled**.

### **Add-On ROM Display Mode**

Set this option to display add-on ROM (read-only memory) messages. The settings for this option are **Force BIOS** and Keep Current. Force BIOS

allows the computer to force a third party BIOS to display during system boot. Keep Current has the system display AMIBIOS information on bootup.

**BootUp Num Lock**

This option is used to select the status of the Number Lock function on your keyboard on bootup. The settings are **On** and Off.

**PS/2 Mouse Support**

This option specifies whether a PS/2 Mouse will be supported. Settings are **Enabled** and Disabled.

**Typematic Rate**

Set this option to select the rate at which the computer repeats a key that is held down. Settings are **Fast** and Slow. Fast: This sets the rate the computer repeats a key to over 20 times per second. Under normal operations, this setting should not be changed. Slow: This sets the rate the computer repeats a key to under 8 times per second.

**System Keyboard**

This option is to let the system know if a keyboard is **Present** or Absent.

**Primary Display**

This option specifies the type of monitor display you have installed on the system. The settings are Absent, **VGA/EGA**, Color 40 x 25, Color 80 x 25 and monochrome.

**Boot to OS/2**

This option can be used to boot the system to an OS/2 operating system. The settings are **No** and Yes.

**Wait for F1 if Error**

This settings for this option are **Enabled** and Disabled. Disabled: This prevents the AMIBIOS to wait on an error for user intervention. This setting should be used if there is a known reason for a BIOS error to appear. An example would be a system administrator must remote boot the system. The computer system does not have a keyboard currently attached. If this setting is set, the system will continue to bootup in to the operating system.

If 'F1' is enabled, the system will wait until the BIOS setup is entered. Enabled: This option allows the system BIOS to wait for any error. If an error is detected, pressing <F1> will enter Setup and the BIOS setting can be adjusted to fix the problem. This normally happens when upgrading the hardware and not setting the BIOS to recognize it.

### Hit "DEL" Message Display

This option tells the system to display or not display the "Hit Delete to Enter Setup" message. The settings are **Enabled** and Disabled.

### Processor Serial Number

This option allows the operating system and applications to be able to read the CPU serial number from your CPUs. The settings are Enabled and **Disabled**. (\*Note: This option is not available for Intel Celeron Processors because these processors do not contain a processor serial number.)

### Internal Cache

This option is for enabling or disabling the internal CPU L1 cache. Settings include Disabled, Write-Thru, **Write-Back** and Reserved. Disabled: This option prevents the system from using the internal CPU L1 cache. This setting should be used to slow the computer system down or to troubleshoot error messages. Write-Thru: This option allows the computer system to use the internal CPU L1 cache as Write-Through cache. Write-Through cache is slower than Write-Back cache. It performs write operations to the internal L1 CPU cache and system memory simultaneously. Write-Back: This option allows the computer system to use the internal CPU L1 cache as Write-Back cache. Write-Back cache is faster than Write-Through cache. Write-Back cache is a caching method in which modifications to data in the cache aren't copied to the cache source until absolutely necessary. Write-back caching is available on all CPUs supported by this BIOS. With these CPUs, write operations stored in the L1 cache aren't copied to main memory until absolutely necessary. This is the default setting.

### System BIOS Cacheable

This option enables you to move the system BIOS to the memory cache to improve performance. Settings are **Enabled** and Disabled.

## **Event Log Configuration**

### **Event Logging**

This option **Enables** or Disables the logging of events. You can use this screen to select options for the Event Log Configuration Settings. You can access sub screens to view the event log and mark all events as read. Use the up and down arrow keys to select an item, and the plus (+) and minus (-) keys to change the option setting. The settings are described on the following pages. The screen is shown below.

### **ECC Event Logging**

This option Enables or **Disables** the logging of ECC events. The events logged by AMIBIOS are post errors such as a bad BIOS, floppy errors, or hard drive errors.

### **View Event Log**

Highlighting this and pressing <Enter> will allow you to view the unread events from the event log area.

### **Mark All Events As Read**

Highlighting [OK] and pressing <Enter> will mark all events in the log area as having been read. The settings are OK and **Cancel**.

## **Peripheral Device Configuration**

### **Onboard SCSI option-ROM**

This option allows you to **Enable** or Disable booting up the system from an onboard SCSI device.

### **Onboard LAN1 option-ROM**

This option allows you to Enable or **Disable** booting up the system from an onboard LAN1 device (a PXE feature).

### **Onboard LAN2 option-ROM**

This option allows you to Enable or **Disable** booting up the system from an onboard LAN2 device (a PXE feature).

### **Power Lost Control**

This option determines how the system will respond when power is reapplied after a power loss condition. Choose **Enabled** to automatically start up the system when power is reapplied. Disabled Off means you must push the main power button to restart the system after power is restored.

## **System Health Monitor**

The BIOS continuously monitors the health of your system by measuring certain voltage levels and temperatures.

### **CPU1 Current Temperature/CPU2 Current Temperature**

This reading displays the real-time temperatures of CPU1 and CPU2.

### **System Overheat Warning**

This option allows you to **Enable** or Disable a system overheat warning signal, used to notify you in the event of a dangerous rise in heat levels.

### **Overheat Warning Temperature**

This option allows you to specify the temperature threshold that, when exceeded, will trigger the overheat warning alarm.

The rest of the System Health Monitor menu lists various voltages and temperatures as they are currently being measured. These include CPU temperature, CPU voltage, the rpms of the CPU, chassis and thermal control fans as well as various other voltages.

## **Remote Access Configuration**

### **Remote Access**

This option allows the user to redirect the console (display) through the COM port when enabled. This is useful when two computers are hooked up to a single monitor. When enabled, the user can toggle the display from one system to the other using the <Tab> key. The function keys are disabled when this setting is enabled. The settings are Serial (ANSI) and **Disabled**.

## 4-5 Chipset Setup

Choose Chipset Setup from the AMIBIOS Setup Utility main menu. The screen is shown below. All Chipset Setup options are described following the screen.

BIOS SETUP UTILITY							
Main	Advanced	Chipset	PCIPnP	Power	Boot	Security	Exit
Write Combining for P6 to PCI		[Enabled]					
Act to DeAct		[6 Clks]					
Act to Read/Write		[3 Clks]					
RA Cycle Time		[8 Clks]					
SDRAM CAS Latency		[CAS Latency 3]					
Memory Auto Precharge		[Disabled]					
SDRAM Fast Timing		[11-1-1]					
Memory Writing Posting		[Enabled]					
Fast ECC Enable		[Disabled]					
Scrubbing Enable		[Disabled]					
AGP Device Address Space Size		[32 MB]					↔ Select Screen
AGP Operations		[Enabled]					↑↓ Select Item
MPS 1.4 Support		[Enabled]					+ - Change Option
EMM 386 Support		[Disabled]					F1 General Help
Watchdog Timer		[Disabled]					F10 Save and Exit
							ESC Exit
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### Write Combining for P6-to-PCI

This settings for this option are Disabled and **Enabled**. Select "Enabled" to enable the function of Write Combining for P6-to-PCI.

### Act to Deact

This settings for this option are **6 Clks** and 5 Clks.

### Act to Read/Write

This settings for this option are **3 Clks** and 2 Clks.

### RAS Precharge Time

This option defines the RAS precharge time. Settings are **3 Clks** and 2 Clks.

**RAS Cycle Time**

This option defines the RAS cycle time. Settings include 10 Clks, 9 Clks, **8 Clks** and 7 Clks.

**SDRAM CAS Latency**

This option defines the SDRAM CAS Latency settings. CAS stands for Column Address Strobe. Settings include **CAS Latency 3** and CAS Latency 2.

**Memory Auto Precharge**

The settings are **Enabled** and Disabled.

**SDRAM Fast Timing**

This option defines the Fast timing settings for SDRAM . Settings include 11-1-1 and **10-1-1-1**.

**Memory Writing Posting**

The settings are **Enabled** and Disabled.

**Fast ECC Enable**

The settings are Enabled and **Disabled**.

**Scrubbing Enable**

The settings are Enabled and **Disabled**.

**AGP Device Address Space Size**

This settings for this option are **32MB**, 64MB, 128MB, 256MB and 512MB.

**AGP Operations**

This settings for this option are **Enabled** and Disabled.

**MPS 1.4 Support**

The settings for this option are **Enabled** and Disabled.

**EMM 386**

This settings for this option are Enabled and **Disabled**.

**Watchdog Timer**

The settings for this option are **Disabled**, 2 minutes, 5 minutes, 10 minutes and 15 minutes.

**4-6 PCI PnP Setup**

Choose PCI/PnP Setup from the AMIBIOS Setup main menu. All PCI/PnP options are described in this section. The PCI/PnP Setup screen is shown below.

BIOS SETUP UTILITY							
Main	Advanced	Chipset	PCI/PnP	Power	Boot	Security	Exit
Plug & Play O/S			[No]				
Reset Config Data			[No]				
PCI Latency Timer			[64]				
Allocate IRQ to VGA			[Yes]				
Palette Snooping			[Disabled]				
PCI IDE BusMaster			[Disabled]				
USB Controller			[Enabled]				
			[Disabled]				
IRQ3			[Available]				
IRQ4			[Available]				
IRQ5			[Available]				
IRQ7			[Available]				
IRQ9			[Available]				
IRQ10			[Available]				
IRQ11			[Available]				
IRQ14			[Available]				
IRQ15			[Available]				
						No: lets the BIOS configure all the devices in the system. Yes: lets the operating system configure Plug and Play (PnP) devices not required for boot if your system has a Plug and Play operating system.	
						↔ Select Screen ↑↓ Select Item +- Change Option F1 General Help F10 Save and Exit ESC Exit	
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**Plug & Play O/S**

The settings for this option are Yes and **No**. Selecting Yes will allow the operating system to configure PnP devices not required for setup (provided your system has an O/S that supports PnP devices). Selecting No lets BIOS configure PnP devices.

### Reset Configuration Data

Choosing the Yes setting will cause the PnP configuration data in the BIOS to be cleared on the next boot up. Choosing the **No** setting does not force PnP data to be cleared on the next boot.

### PCI Latency Timer

This option specifies the latency timing of the PCI clocks for all PCI devices. Settings include 32, **64**, 96, 128, 160, 192, 224 and 248 PCI clocks.

### Allocate IRQ to PCI VGA

This option lets you allocate an interrupt request (IRQ) to the PCI VGA adapter card (if used). The settings are **Yes** and No.

### Palette Snooping

When enabled, this option informs PCI devices that an ISA graphics device is installed. The settings are **Disabled** and Enabled. This does not necessarily indicate a physical ISA adapter card. The graphics chipset can be mounted on a PCI card. Always check with your adapter card manuals first, before modifying the default settings in the BIOS.

### PCI IDE BusMaster

The settings for this option are **Disabled** and Enabled. Enable to specify that the IDE controller on the PCI bus has bus mastering capabilities.

### USB Function

The settings for this option are Disabled and **Enabled**. Disabled prevents the use of the USB ports and Enabled allows the use of the USB ports.

### IRQ 3

### IRQ 4

### IRQ 5

### IRQ 7

### IRQ 9

**IRQ 10****IRQ 11****IRQ 14****IRQ 15**

The settings for the above options are **Available** and **Reserved**. Available allows the specified IRQ to be available for use by PCI/PnP devices. Reserved means the specified IRQ is reserved for use by Legacy ISA devices.

## 4-7 Power Setup

Choose Power Setup from the AMIBIOS Setup main menu. All Power Setup options are described in this section. The Power Setup screen is shown below.

BIOS SETUP UTILITY							
Main	Advanced	Chipset	PCIPnP	Power	Boot	Security	Exit
ACPI Aware O/S				[No]			
Power Button Mode				[On/Off]			
Suspend Time Out (Minutes)				[Off]			
PME Resume				[Disabled]			
RI/WOR Resume				[Disabled]			
Chassis Intrusion Support				[Disabled]			
							↔ Select Screen
							↑↓ Select Item
							+ - Change Option
							F1 General Help
							F10 Save and Exit
							ESC Exit
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### **ACPI Aware O/S**

This option allows the system to utilize Intel's ACPI (Advanced Configuration and Power Interface) specification. Settings are **No** and **Yes**. DOS®, Windows 3.x®, and Windows NT® are examples of non-ACPI aware operating systems. Windows 95®, Windows 98®, Windows ME® and Windows 2000® are examples of ACPI aware operating systems.

### **Power Button Mode**

This option allows you to specify how the power button will function. **On/Off** allows it to function normally. Choosing **Suspend** allows you to put the system in a suspend (sleep) state when depressing the button.

### **Suspend Timeout**

This option specifies if BIOS is to monitor for display activity when in a power saving state. The settings include **Off**, 1, 2, 3, 4, 5, 6, 7, 8, 9 and 10 (minutes).

### **PME Resume**

This allows you to wake up the system from a PME device. The settings for this option **Disabled** and **Enabled**.

### **RI/WOR Resume**

This option allows the system to resume the Ring Indicator/Wake-on-Ring function. The settings for this option **Disabled** and **Enabled**.

### **Chassis Intrusion Support**

This option allows BIOS to help you support the chassis intrusion function. When **Enabled**, the system will freeze if a chassis intrusion is detected. The settings are **Enabled** and **Disabled**.

## 4-8 Boot Setup

Choose Boot Setup from the AMIBIOS Setup main menu. All Boot Setup options are described in this section. The Boot Setup screen is shown below.

BIOS SETUP UTILITY							
Main	Advanced	Chipset	PCIPnP	Power	Boot	Security	Exit
> <u>Boot Device Priority</u> > Hard Disk Drives > Removable Devices > ATAPI CDROM Drives						↔ Select Screen ↑↓ Select Item Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit	
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### Boot Device Priority

#### 1st Boot Device

This option is used to specify the order of the boot sequence that will be followed from the available system devices. The settings for the 1st Boot Device are **Removable Device**, ATAPI CDROM, Hard Drive and Disabled.

#### 2nd Boot Device

The settings for the 2nd Boot Device are Removable Device, **ATAPI CDROM**, Hard Drive and Disabled.

### **3rd Boot Device**

The settings for the 3rd Boot Device are Removable Device, ATAPI CDROM, **Hard Drive** and Disabled.

### **Hard Disk Drives**

Use this screen to view the boot sequency of hard drives that have been auto-detected or entered manually on your system.

### **Removable Devices**

Use this screen to view the boot sequency of the removeable devices that have been auto-detected or entered manually on your system.

### **ATAPI CDROM Drives**

Use this screen to view the boot sequency ofthe ATAPI CDROM drives that have been auto-detected or entered manually on your system.

## 4-9 Security Setup

Choose Security Setup from the AMIBIOS Setup main menu. All Security Setup options are described in this section. The Security Setup screen is shown below.

BIOS SETUP UTILITY							
Main	Advanced	Chipset	PCIPnP	Power	Boot	Security	Exit
Supervisor Password :						Not Installed	
User Password :						Not Installed	
> <u>Change Supervisor Password</u>							
> Change User Password							
> Clear User Password							
Boot Sector Virus Protection						[Disabled]	
						Install or Change the password.	
						↔ Select Screen	
						↑↓ Select Item	
						Enter Go to Sub Screen	
						F1 General Help	
						F10 Save and Exit	
						ESC Exit	
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### Supervisor Password

### User Password

AMIBIOS provides both Supervisor and User password functions. If you use both passwords, the Supervisor password must be set first. The system can be configured so that all users must enter a password every time the system boots or when AMIBIOS Setup is executed, using either or both the Supervisor password or User password. The Supervisor and User passwords activate two different levels of password security. If you select password support, you are prompted for a 1 – 6 character password. Type the password on the keyboard. The password does not appear on the screen when typed. Make sure you write it down. If you forget it, you must clear CMOS and reconfigure. **Remember your Password!** Keep a record of the new password when the password is changed. If you forget the password, you must erase the system configuration information in CMOS.

### **Change Supervisor Password**

This option allows you to change a supervisor password that was entered previously.

### **Change User Password**

This option allows you to change a user password that was entered previously.

### **Clear User Password**

Use this option to clear the user password so that it is not required to be entered when the system boots up.

### **Boot Sector Virus Protection**

This option allows you to enable or disable a virus detection program to protect the boot sector of your hard disk drive. The settings for this option **Disabled** and Enabled. If Enabled, AMIBIOS will display a warning when any program (or virus) issues a Disk Format command or attempts to write to the boot sector of the hard disk drive.

## 4-10 Exit Setup

Choose Exit Setup from the AMIBIOS Setup main menu. All Exit Setup options are described in this section. The Exit Setup screen is shown below.

BIOS SETUP UTILITY							
Main	Advanced	Chipset	PCIPnP	Power	Boot	Security	Exit
> <u>Exit Saving Changes</u> > Exit Discarding Changes > Load Optimal Defaults > Load Fail-Safe Defaults > Discard Changes							Exit system setup with saving the changes.
							↔ Select Screen ↑↓ Select Item Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit
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### Exit Saving Changes

Highlighting this setting and then pressing <Enter> will save any changes you made in the BIOS Setup program and then exit. Your system should then continue with the boot up procedure.

### Exit Discarding Changes

Highlighting this setting and then pressing <Enter> will ignore any changes you made in the BIOS Setup program and then exit. Your system should then continue with the boot up procedure.

### **Load Optimal Defaults**

Highlighting this setting and then pressing <Enter> provides the optimum performance settings for all devices and system features.

### **Load Failsafe Defaults**

Highlighting this setting and then pressing <Enter> provides the safest set of parameters for the system. Use them if the system is behaving erratically.

### **Discard Changes**

Highlighting this setting and then pressing <Enter> will ignore any changes you made in the BIOS Setup program but will not exit the BIOS Setup program.

**Notes**

## Appendix A

# BIOS Error Beep Codes & Messages

During the POST (Power-On Self-Test) routines, which are performed each time the system is powered on, errors may occur.

**Non-fatal errors** are those which, in most cases, allow the system to continue the boot-up process. The error messages normally appear on the screen.

**Fatal errors** are those which will not allow the system to continue the boot-up procedure. If a fatal error occurs, you should consult with your system manufacturer for possible repairs.

These fatal errors are usually communicated through a series of audible beeps. The numbers on the fatal error list, on the following page, correspond to the number of beeps for the corresponding error. All errors listed, with the exception of Beep Code 8, are fatal errors.

## AMIBIOS Error Beep Codes

<b>Beep Code</b>	<b>Error Message</b>	<b>Description</b>
1 beep	Refresh	Circuits have been reset. (Ready to power up.)
6 beeps	Memory error	No memory detected in system
8 beeps	Display memory read/write error	Video adapter missing or with faulty memory

## Appendix B

### AMIBIOS POST Checkpoint Codes

When AMIBIOS performs the Power On Self Test, it writes diagnostic codes checkpoint codes to I/O port 0080h. If the computer cannot complete the boot process, diagnostic equipment can be attached to the computer to read I/O port 0080h.

#### B-1 Uncompressed Initialization Codes

The uncompressed initialization checkpoint codes are listed in order of execution:

<b>Checkpoint</b>	<b>Code Description</b>
D0h	The NMI is disabled. Power on delay is starting. Next, the initialization code checksum will be verified.
D1h	Initializing the DMA controller, performing the keyboard controller BAT test, starting memory refresh, and entering 4 GB flat mode next.
D3h	Starting memory sizing next.
D4h	Returning to real mode. Executing any OEM patches and setting the Stack next.
D5h	Passing control to the uncompressed code in shadow RAM at E000:0000h. The initialization code is copied to segment 0 and control will be transferred to segment 0.
D6h	Control is in segment 0. Next, checking if <Ctrl> <Home> was pressed and verifying the system BIOS checksum. If either <Ctrl> <Home> was pressed or the system BIOS checksum is bad, next will go to checkpoint code E0h. Otherwise, going to checkpoint code D7h.

## B-2 Bootblock Recovery Codes

The bootblock recovery checkpoint codes are listed in order of execution:

<b>Checkpoint</b>	<b>Code Description</b>
E0h	The onboard floppy controller if available is initialized. Next, beginning the base 512 KB memory test.
E1h	Initializing the interrupt vector table next.
E2h	Initializing the DMA and Interrupt controllers next.
E6h	Enabling the floppy drive controller and Timer IRQs. Enabling internal cache memory.
Edh	Initializing the floppy drive.
Eeh	Looking for a floppy diskette in drive A:. Reading the first sector of the diskette.
Efh	A read error occurred while reading the floppy drive in drive A:.
F0h	Next, searching for the AMIBOOT.ROM file in the root directory.
F1h	The AMIBOOT.ROM file is not in the root directory.
F2h	Next, reading and analyzing the floppy diskette FAT to find the clusters occupied by the AMIBOOT.ROM file.
F3h	Next, reading the AMIBOOT.ROM file, cluster by cluster.
F4h	The AMIBOOT.ROM file is not the correct size.
F5h	Next, disabling internal cache memory.
FBh	Next, detecting the type of flash ROM.
FCh	Next, erasing the flash ROM.
FDh	Next, programming the flash ROM.
FFh	Flash ROM programming was successful. Next, restarting the system BIOS.

## B-3 Uncompressed Initialization Codes

The following runtime checkpoint codes are listed in order of execution.

These codes are uncompressed in F0000h shadow RAM.

<b>Checkpoint</b>	<b>Code Description</b>
03h	The NMI is disabled. Next, checking for a soft reset or a power on condition.
05h	The BIOS stack has been built. Next, disabling cache memory.
06h	Uncompressing the POST code next.
07h	Next, initializing the CPU and the CPU data area.
08h	The CMOS checksum calculation is done next.
0Ah	The CMOS checksum calculation is done. Initializing the CMOS status register for date and time next.

---

0Bh	The CMOS status register is initialized. Next, performing any required initialization before the keyboard BAT command is issued.
0Ch	The keyboard controller input buffer is free. Next, issuing the BAT command to the keyboard controller.
0Eh	The keyboard controller BAT command result has been verified. Next, performing any necessary initialization after the keyboard controller BAT command test.
0Fh	The initialization after the keyboard controller BAT command test is done. The keyboard command byte is written next.
10h	The keyboard controller command byte is written. Next, issuing the Pin 23 and 24 blocking and unblocking command.
11h	Next, checking if <End or <Ins> keys were pressed during power on. Initializing CMOS RAM if the <i>Initialize CMOS RAM in every boot</i> AMIBIOS POST option was set in AMIBCP or the <End> key was pressed.
12h	Next, disabling DMA controllers 1 and 2 and interrupt controllers 1 and 2.
13h	The video display has been disabled. Port B has been initialized. Next, initializing the chipset.
14h	The 8254 timer test will begin next.
19h	The 8254 timer test is over. Starting the memory refresh test next.
1Ah	The memory refresh line is toggling. Checking the 15 second on/off time next.
2Bh	Passing control to the video ROM to perform any required configuration before the video ROM test.
2Ch	All necessary processing before passing control to the video ROM is done. Looking for the video ROM next and passing control to it.
2Dh	The video ROM has returned control to BIOS POST. Performing any required processing after the video ROM had control.
23h	Reading the 8042 input port and disabling the MEGAKEY Green PC feature next. Making the BIOS code segment writable and performing any necessary configuration before initializing the interrupt vectors.
24h	The configuration required before interrupt vector initialization has completed. Interrupt vector initialization is about to begin.

<b>Checkpoint</b>	<b>Code Description</b>
25h	Interrupt vector initialization is done. Clearing the password if the POST DIAG switch is on.
27h	Any initialization before setting video mode will be done next.
28h	Initialization before setting the video mode is complete. Configuring the monochrome mode and color mode settings next.
2Ah	Bus initialization system, static, output devices will be done next, if present. See the last page for additional information.
2Eh	Completed post-video ROM test processing. If the EGA/VGA controller is not found, performing the display memory read/write test next.
2Fh	The EGA/VGA controller was not found. The display memory read/write test is about to begin.
30h	The display memory read/write test passed. Look for retrace checking next.
31h	The display memory read/write test or retrace checking failed. Performing the alternate display memory read/write test next.
32h	The alternate display memory read/write test passed. Looking for alternate display retrace checking next.
34h	Video display checking is over. Setting the display mode next.
37h	The display mode is set. Displaying the power on message next.
38h	Initializing the bus input, IPL, general devices next, if present. See the last page of this chapter for additional information.
39h	Displaying bus initialization error messages. See the last page of this chapter for additional information.
3Ah	The new cursor position has been read and saved. Displaying the <i>Hit &lt;DEL&gt;</i> message next.
3Bh	The <i>Hit &lt;DEL&gt;</i> message is displayed. The protected mode memory test is about to start.
40h	Preparing the descriptor tables next.
42h	The descriptor tables are prepared. Entering protected mode for the memory test next.
43h	Entered protected mode. Enabling interrupts for diagnostics mode next.
44h	Interrupts enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0 next.
45h	Data initialized. Checking for memory wraparound at 0:0 and finding the total system memory size next.
46h	The memory wraparound test is done. Memory size calculation has been done. Writing patterns to test memory next.
47h	The memory pattern has been written to extended memory. Writing patterns to the base 640 KB memory next.

<b>Checkpoint</b>	<b>Code Description</b>
48h	Patterns written in base memory. Determining the amount of memory below 1 MB next.
49h	The amount of memory below 1 MB has been found and verified. Determining the amount of memory above 1 MB memory next.
4Bh	The amount of memory above 1 MB has been found and verified. Checking for a soft reset and clearing the memory below 1 MB for the soft reset next. If this is a power on situation, going to checkpoint 4Eh next.
4Ch	The memory below 1 MB has been cleared via a soft reset. Clearing the memory above 1 MB next.
4Dh	The memory above 1 MB has been cleared via a soft reset. Saving the memory size next. Going to checkpoint 52h next.
4Eh	The memory test started, but not as the result of a soft reset. Displaying the first 64 KB memory size next.
4Fh	The memory size display has started. The display is updated during the memory test. Performing the sequential and random memory test next.
50h	The memory below 1 MB has been tested and initialized. Adjusting the displayed memory size for relocation and shadowing next.
51h	The memory size display was adjusted for relocation and shadowing. Testing the memory above 1 MB next.
52h	The memory above 1 MB has been tested and initialized. Saving the memory size information next.
53h	The memory size information and the CPU registers are saved. Entering real mode next.
54h	Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next.
57h	The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next.
58h	The memory size was adjusted for relocation and shadowing. Clearing the <i>Hit &lt;DEL&gt;</i> message next.
59h	The <i>Hit &lt;DEL&gt;</i> message is cleared. The <i>&lt;WAIT...&gt;</i> message is displayed. Starting the DMA and interrupt controller test next.

<b>Checkpoint</b>	<b>Code Description</b>
60h	The DMA page register test passed. Performing the DMA Controller 1 base register test next.
62h	The DMA controller 1 base register test passed. Performing the DMA controller 2 base register test next.
65h	The DMA controller 2 base register test passed. Programming DMA controllers 1 and 2 next.
66h	Completed programming DMA controllers 1 and 2. Initializing the 8259 interrupt controller next.
67h	Completed 8259 interrupt controller initialization.
7Fh	Extended NMI source enabling is in progress.
80h	The keyboard test has started. Clearing the output buffer and checking for stuck keys. Issuing the keyboard reset command next.
81h	A keyboard reset error or stuck key was found. Issuing the keyboard controller interface test command next.
82h	The keyboard controller interface test completed. Writing the command byte and initializing the circular buffer next.
83h	The command byte was written and global data initialization has completed. Checking for a locked key next.
84h	Locked key checking is over. Checking for a memory size mismatch with CMOS RAM data next.
85h	The memory size check is done. Displaying a soft error and checking for a password or bypassing WINBIOS Setup next.
86h	The password was checked. Performing any required programming before WINBIOS Setup next.
87h	The programming before WINBIOS Setup has completed. Uncompressing the WINBIOS Setup code and executing the AMIBIOS Setup or WINBIOS Setup utility next.
88h	Returned from WINBIOS Setup and cleared the screen. Performing any necessary programming after WINBIOS Setup next.
89h	The programming after WINBIOS Setup has completed. Displaying the power on screen message next.
8Bh	The first screen message has been displayed. The <WAIT...> message is displayed. Performing the PS/2 mouse check and extended BIOS data area allocation check next.
8Ch	Programming the WINBIOS Setup options next.
8Dh	The WINBIOS Setup options are programmed. Resetting the hard disk controller next.
8Fh	The hard disk controller has been reset. Configuring the floppy drive controller next.
91h	The floppy drive controller has been configured. Configuring the hard disk drive controller next.

<b>Checkpoint</b>	<b>Code Description</b>
95h	Initializing the bus option ROMs from C800 next. See the last page of this chapter for additional information.
96h	Initializing before passing control to the adaptor ROM at C800.
97h	Initialization before the C800 adaptor ROM gains control has completed. The adaptor ROM check is next.
98h	The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control.
99h	Any initialization required after the option ROM test has completed. Configuring the timer data area and printer base address next.
9Ah	Set the timer and printer base addresses. Setting the RS-232 base address next.
9Bh	Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test next.
9Ch	Required initialization before the Coprocessor test is over. Initializing the Coprocessor next.
9Dh	Coprocessor initialized. Performing any required initialization after the Coprocessor test next.
9Eh	Initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next.
A2h	Displaying any soft errors next.
A3h	The soft error display has completed. Setting the keyboard typematic rate next.
A4h	The keyboard typematic rate is set. Programming the memory wait states next.
A5h	Memory wait state programming is over. Clearing the screen and enabling parity and the NMI next.
A7h	NMI and parity enabled. Performing any initialization required before passing control to the adaptor ROM at E000 next.
A8h	Initialization before passing control to the adaptor ROM at E000h completed. Passing control to the adaptor ROM at E000h next.
A9h	Returned from adaptor ROM at E000h control. Performing any initialization required after the E000 option ROM had control next.
Aah	Initialization after E000 option ROM control has completed. Displaying the system configuration next.
Abh	Uncompressing the DMI data and executing DMI POST initialization next.
B0h	The system configuration is displayed.
B1h	Copying any code to specific areas.
00h	Code copying to specific areas is done. Passing control to INT 19h boot loader next.

**Notes**