SUPER®

SUPER X5DPA-G
SUPER X5DPA-GG

USER'S MANUAL

Revision 1.0b

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Printed in the United States of America

Preface

About This Manual

This manual is written for system integrators, PC technicians and knowledgeable PC users. It provides information for the installation and use of the SUPER X5DPA-G/X5DPA-GG mainboard. The SUPER X5DPA-G/X5DPA-GG supports single or dual Intel® 604 and 603-pin Xeon™ processors at up to 3.06 GHz at a 533/400 MHz front side bus. Please refer to the support section of our web site (http://www.supermicro.com/TechSupport.htm) for a complete listing of supported processors. This product is intended to be professionally installed.

Manual Organization

Chapter 1 begins with a checklist of what should be included in your mainboard box, describes the features, specifications and performance of the motherboard and provides detailed information about the chipset.

Chapter 2 begins with instructions on handling static-sensitive devices. Read this chapter when you want to install the processor and DIMM memory modules and when mounting the mainboard in the chassis. Also refer to this chapter to connect the floppy and hard disk drives, SCSI drives, the IDE interfaces, the parallel and serial ports, the keyboard and mouse, the power supply and various control panel buttons and indicators.

If you encounter any problems, see **Chapter 3**, which describes troubleshooting procedures for the video, the memory and the setup configuration stored in CMOS. For quick reference, a general FAQ [Frequently Asked Questions] section is provided. Instructions are also included for contacting technical support. In addition, you can visit our web site (at www.supermicro.com/techsupport.htm) for more detailed information.

Chapter 4 includes an introduction to BIOS and provides detailed information on running the CMOS Setup utility.

Appendix A gives information on BIOS POST messages.

Appendix B provides BIOS POST codes.

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Chapter 2: Installation

Chapter 3: Troubleshooting

Chapter 4: BIOS

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Chapter 1
Introduction

1-1 Overview

Checklist

Congratulations on purchasing your computer motherboard from an acknowledged leader in the industry. Supermicro boards are designed with the utmost attention to detail to provide you with the highest standards in quality and performance.

Please check that the following items have been included with your motherboard. If anything listed here is damaged or missing, contact your retailer.

One (1) Supermicro Mainboard

One (1) ribbon cable for IDE devices

One (1) floppy ribbon cable

One (1) USB cable

One (1) COM Port Cable with Bracket

One (1) I/O backpanel shield

One (1) Supermicro CD or diskettes containing drivers and utilities

One (1) User's/BIOS Manual

Two (2)CPU/Heatsink Plates (SKT-120-P) and two (2) heatsink retention clips (SKT-095-604 E)

Contacting Supermicro

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NOTES

Figure 1-1. SUPER X5DPA-G Image

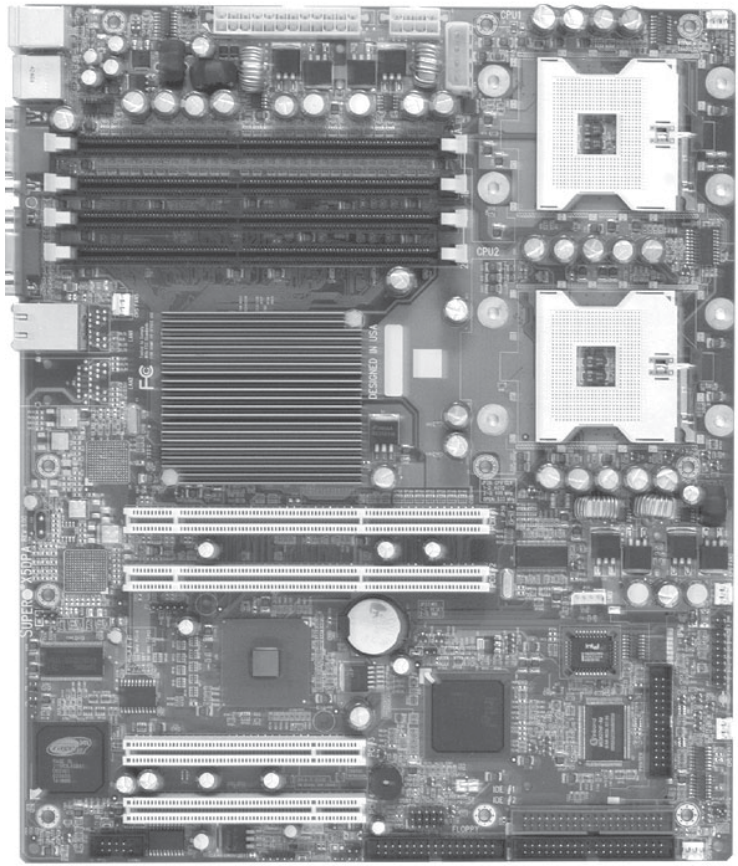


Figure 1-2. SUPER X5DPA-GG Image

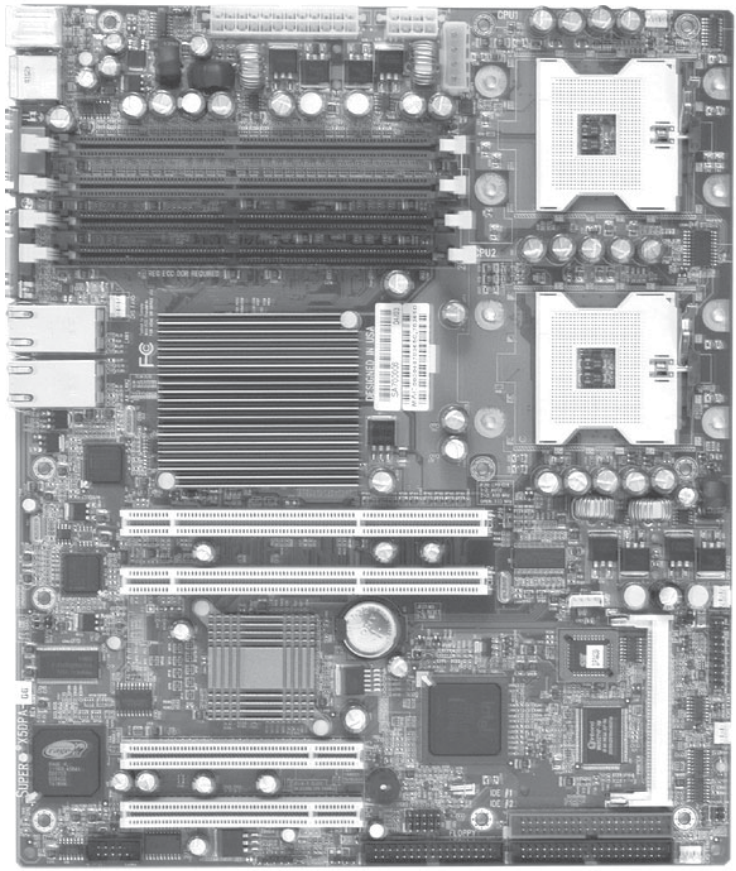
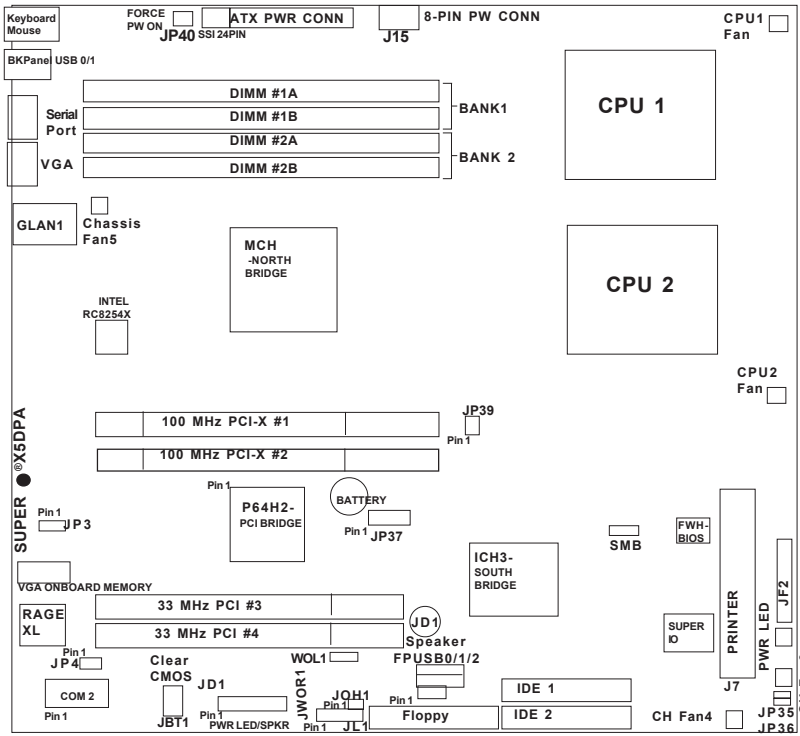


Figure 1-3. SUPER X5DPA-G Layout*
(not drawn to scale)



Notes:

1. The CPU sockets are designed for the 604-Pin Xeon Processors; however, the 603-Pin CPUs are also supported. When one CPU is used, please install it in CPU Socket #1.

2. DIMM memory modules have to be used in pairs. When one pair of DIMMs are used, please install them in the Bank #1.

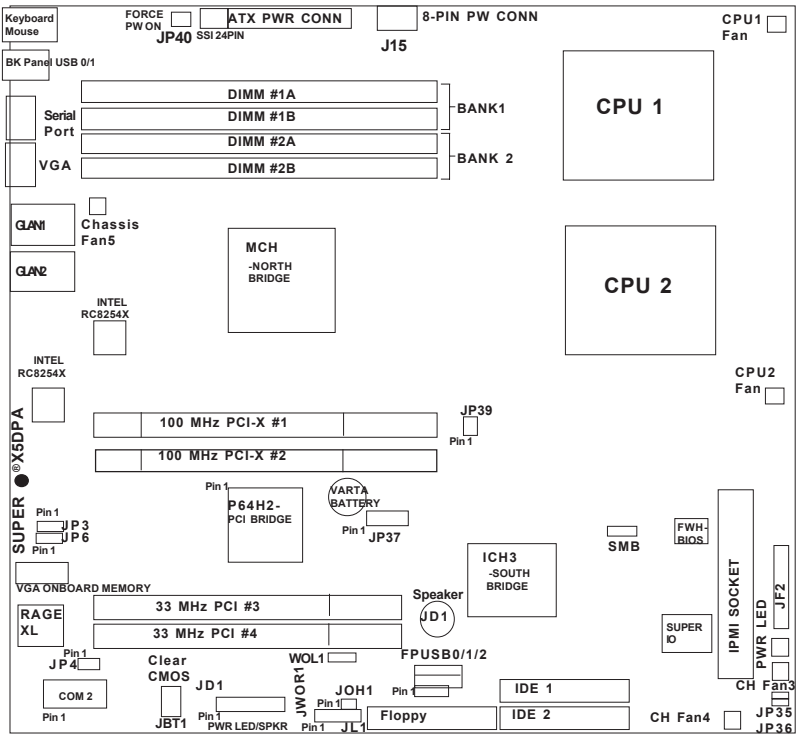
X5DPA-G Quick Reference

Jumper	Description	Default Setting
JBT1	CMOS Clear	See Jumper Section
JD1	PWR LED/Speaker Header	Pins 6-7 (Onboard Speaker)
JP3	GLAN1 Enable/Disable	Pins 1-2 (Enabled)
JP4	VGA Enable/Disable	Pins 1-2 (Enabled)
JP37	Watch Dog (Reset/NMI)	Pins 2-3 NMI(*Note)
JP39	CPU Clock	Pins 1-2 (Auto)
JP40	Force Power On	Open (Disabled)

Connector	Description
ATX PWR CONN	Primary ATX Power Connector
DIMM#1A-DIMM#2B	Memory (RAM) Slots
CPU/CHASSIS FANS	CPU/Chassis Fan Headers
LAN1	GLAN1(Gigabit Ethernet Port 1)
J2/J3	IDE#1(J2), IDE#2(J3) HDD Connectors
J4	VGA Connector
J7	Printer Connector
JP7	Floppy Disk Drive Connector
J8, J26	COM1(SerialPort1-J8),COM2(SerialPort2-J26)
J10,J11	Back Panel USB 0/1Ports (J10:USB 0, J11: USB 1)
JD2, J27, USB5	Front Panel USB Ports (JD2: USB2/3, J27:USB4), USB5
J15	Secondary ATX Power (8-Pin) Connector
JF2	Front Control Panel Connector
JL1	Chassis Intrusion Header
JOH1	Overheat LED
J28	PS/2 Keyboard & PS/2 Mouse
JP35	Keylock Switch Connector
JP36	Alarm Reset Switch
JWOR1	Wake-on-Ring Header
WOL1	Wake-on-LAN Header

(*Note: NMI: Non Maskable Interrupt)

Figure 1-3. SUPER X5DPA-GG Layout*
(not drawn to scale)



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X5DPA-GG Quick Reference

Jumper	Description	Default Setting
JBT1	CMOS Clear	See Jumper Section
JD1	PWR LED/Speaker Header	Pins 6-7 (Onboard Speaker)
JP3	GLAN1 Enable/Disable	Pins 1-2 (Enabled)
JP6	GLAN2 Enable/Disable	Pins 1-2 (Enabled)
JP4	VGA Enable/Disable	Pins 1-2 (Enabled)
JP37	Watch Dog (Reset/NMI*)	Pins 2-3 NMI(*Note)
JP39	CPU Clock	Pins 1-2 (Auto)
JP40	Force Power ON	Open (Disabled)

Connector	Description
ATX PWR CONN	Primary ATX Power Connector
DIMM#1A-DIMM#2B	Memory (RAM) Slots
CPU/Chassis FAN	CPU/Chassis Fan Headers (5)
LAN1	GLAN1(Gigabit Ethernet Port 1)
LAN2	GLAN2(Gigabit Ethernet Port 2)
J2/J3	IDE#1(J2), IDE#2(J3) HDD Connectors
J4	VGA Connector
JP7	Floppy Disk Drive Connector
J8, J26	COM1(SerialPort1-J8),COM2(SerialPort2-J26)
J10,J11	Back Panel USB 0/1Ports (J10:USB 0, J11: USB 1)
JD2, J27,USB5	Front Panel USB Ports (JD2: USB2/3, J27:USB4),USB5
J15	Secondary ATX Power (8-Pin) Connector
J22	IPMI Socket
JF2	Front Control Panel Connector
JL1	Chassis Intrusion Header
JOH1	Overheat LED
J28	PS/2 Keyboard & PS/2 Mouse
JP35	Keylock Switch Connector
JP36	Alarm Reset Switch
JWOR1	Wake-on-Ring Header
WOL	Wake-on-LAN Header

(*Note: NMI: Non Maskable Interrupt)

Motherboard Features

CPU

- Single or dual Intel® 604-Pin Xeon™ processors of up to 3.06GHz at a 533/400 MHz front side (system) bus speed. (603-Pin Xeon supported)

  Note: Please refer to the support section of our web site for a complete listing of supported processors (http://www.supermicro.com/TechSupport.htm).

Memory

- Four 184-pin DIMM sockets supporting up to 8 GB of registered ECC DDR-266/200 SDRAM

  Note: Interleaved memory; requires memory modules to be installed in pairs. DDR-266 memory must be used with 533 MHz FSB speed processors. (*If DDR-266 memory is used with 400 MHz FSB speed processors, it will run at 200 MHz.)See Section 2-3 for details.

Chipset

- Intel E7501 chipset

Expansion Slots

X5DPA-GG/X5DPA-G

- Two 64-bit, 133/100/66 MHz PCI-X (3.3 V) (*only one slot is available for 133MHz bus PCI-X.)
- Two 32-bit, 33 MHz PCI

BIOS

- 4 Mb AMI Flash ROM
- APM 1.2, DMI 2.1, PCI 2.2, ACPI 1.0, Plug and Play (PnP), SMBIOS 2.3

PC Health Monitoring

- Onboard voltage monitors for CPU cores, 3.3V,+12V,–12V and 3.3V standby
- Fan status monitor with firmware/software on/off control
- CPU/chassis temperature monitors
- Environmental temperature monitor and control
- CPU fan auto-off in sleep mode
- CPU slow-down on temperature overheat
- CPU overheat LED header
- Power-up mode control for recovery from AC power loss
- Auto-switching voltage regulator for CPU core
- System overheat LED and control
- Chassis intrusion detection

- System resource alert

ACPI Features (optional)

- Microsoft OnNow
- Slow blinking LED for suspend state indicator
- Main switch override mechanism

Onboard I/O

- Integrated ATI Rage XL graphics controller
- Intel Gigabit LAN (Ethernet) 8254X controller (* two GLAN ports on X5DPA-GG, one GLAN port on X5DPA-G)
- 2 EIDE Ultra DMA/100 bus master interfaces
- 1 floppy port interface (up to 2.88 MB)
- 2 Fast UART 16550A compatible serial ports
- PS/2 mouse and PS/2 keyboard ports
- Up to 5 USB (Universal Serial Bus) ports
- Parallel port on X5DPA-G

Other

- Internal/external modem ring-on
- Wake-on-LAN (WOL)
- Console redirection
- IPMI (*X5DPA-GG only-optional)

CD/Diskette Utilities

- BIOS flash upgrade utility and device drivers

Dimensions

- ATX: 12" x 10" (304.8 x 254 mm)

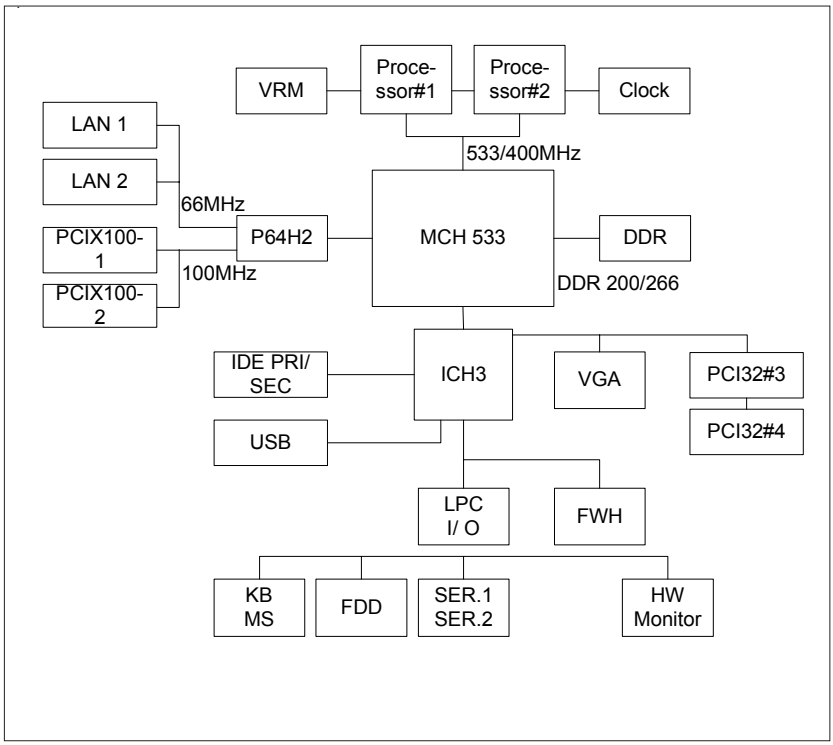


Figure 1-5. X5DPA: Block Diagram

Note: This is a general block diagram. Please see the previous Motherboard Features pages for details on the features of each motherboard.

1-2 Chipset Overview

The Intel E7501 chipset is a high-performance chipset with a performance and feature-set designed for mid-range, dual processor servers. The E7501 chipset consists of four major components: the Memory Controller Hub (MCH), the I/O Controller Hub 3 (ICH3), the PCI-X 64-bit Hub 2.0 (P64H2) and the FW82801CA FIRMWARE Controller.

The MCH has four hub interfaces, one to communicate with the ICH3 and three for high-speed I/O communications. The MCH employs a 144-bit wide memory bus for a DDR-266 memory interface, which provides a total bandwidth of 3.2 GB/s. The ICH3 interface is a 266 MB/sec point-to-point connection using an 8-bit wide, 66 MHz base clock at a 4x data transfer rate. The P64H2 interface is a 1 GB/s point-to-point connection using a 16-bit wide, 66 MHz base clock at a 8x data transfer rate.

The ICH3 I/O Controller Hub provides various integrated functions, including a two-channel UDMA100 bus master IDE controller, USB host controllers, a System Management Bus controller and an AC'97 compliant interface.

The P64H2 PCI-X Hub provides a 16-bit connection to the MCH for high-performance I/O capability and two 64-bit PCI-X interfaces.

1-3 Special Features

ATI Graphics Controller

The X5DPA-G/X5DPA-GG has an integrated ATI video controller based on the Rage XL graphics chip. The Rage XL fully supports sideband addressing and AGP texturing. This onboard graphics package can provide a bandwidth of up to 512 MB/sec over a 32-bit graphics memory bus.

Recovery from AC Power Loss

BIOS provides a setting for you to determine how the system will respond when AC power is lost and then restored to the system. You can choose for the system to remain powered off (in which case you must hit the power switch to turn it back on) or for it to automatically return to a power-on state. See the Power Lost Control setting in the AMI BIOS Utility to change this setting.

1-4 PC Health Monitoring

This section describes the PC health monitoring features of the SUPER X5DPA-G/X5DPA-GG. All have an onboard System Hardware Monitor chip that supports PC health monitoring.

Onboard Voltage Monitors for the CPU Cores,+3.3V,+12V,-12V and +3.3V Standby

An onboard voltage monitor will scan these voltages continuously. Once a voltage becomes unstable, a warning is given or an error message is sent to the screen. Users can adjust the voltage thresholds to define the sensitivity of the voltage monitor.

Fan Status Monitor with Firmware/Software On/Off Control

The PC health monitor can check the RPM status of the cooling fans. The onboard 3-pin CPU and chassis fans are controlled by the power management functions.

Environmental Temperature Control

The thermal control sensor monitors the CPU temperature in real time and will turn on the thermal control fan whenever the CPU temperature exceeds a user-defined threshold. The overheat circuitry runs independently from the CPU. It can continue to monitor for overheat conditions even when the CPU is in sleep mode. Once it detects that the CPU temperature is too high, the Overheat buzzer and the LED will be automatically activated. The onboard chassis thermal circuitry can monitor the overall system temperature and alert users when the chassis temperature is too high.

CPU Fan Auto-Off in Sleep Mode

The CPU fan activates when the power is turned on. It continues to operate when the system enters Standby mode. When in sleep mode, the CPU will not run at full power, thereby generating less heat.

CPU Overheat LED and Control

This feature is available when the user enables the CPU overheat warning function in the BIOS. This allows the user to define an overheat temperature. When this temperature is exceeded, both the overheat buzzer and the warning LED are triggered.

System Resource Alert

This feature is available when used with Intel's LANDesk Client Manager (optional). LDCM is used to notify the user of certain system events. For example, if the system is running low on virtual memory and there is insufficient hard drive space for saving the data, you can be alerted of the potential problem.

Auto-Switching Voltage Regulator for the CPU Core

The auto-switching voltage regulator for the CPU core can support up to 20A current and auto-sense voltage IDs ranging from 1.4V to 3.5V. This will allow the regulator to run cooler and thus make the system more stable.

1-5 ACPI Features

ACPI stands for Advanced Configuration and Power Interface. The ACPI specification defines a flexible and abstract hardware interface that provides a standard way to integrate power management features throughout a PC system, including its hardware, operating system and application software. This enables the system to automatically turn on and off peripherals such as CD-ROMs, network cards, hard disk drives and printers. This also includes consumer devices connected to the PC such as VCRs, TVs, telephones and stereos.

In addition to enabling operating system-directed power management, ACPI provides a generic system event mechanism for Plug and Play and an operating system-independent interface for configuration control. ACPI leverages the Plug and Play BIOS data structures while providing a processor architecture-independent implementation that is compatible with both Windows 2000 and Windows NT 5.0.

Microsoft OnNow

The OnNow design initiative is a comprehensive, system-wide approach to system and device power control. OnNow is a term for a PC that is always on but appears to be off and responds immediately to user or other requests.

Slow Blinking LED for Suspend-State Indicator

When the CPU goes into a suspend state, the chassis power LED will start blinking to indicate that the CPU is in suspend mode. When the user presses any key, the CPU will wake-up and the LED will automatically stop blinking and remain on.

Main Switch Override Mechanism

When an ATX power supply is used, the power button can function as a system suspend button to make the system enter a SoftOff state. The monitor will be suspended and the hard drive will spin down. Depressing the power button again will cause the whole system to wake-up. During the SoftOff state, the ATX power supply provides power to keep the required circuitry in the system alive. In case the system malfunctions and you want to turn off the power, just depress and hold the power button for 4 seconds. This option can be set in the "BIOS features" under the "Advanced Menu."

External Modem Ring-On

Wake-up events can be triggered by a device such as the external modem ringing when the system is in the SoftOff state. Note that external modem ring-on can only be used with an ATX 2.01 (or above) compliant power supply.

Wake-On-LAN (WOL)

Wake-On-LAN is defined as the ability of a management application to remotely power up a computer that is powered off. Remote PC setup, updates and asset tracking can occur after hours and on weekends so that daily LAN traffic is kept to a minimum and users are not interrupted. The motherboards have a 3-pin header (WOL) to connect to the 3-pin header on

a Network Interface Card (NIC) that has WOL capability. Wake-On-LAN must be enabled in BIOS. Note that Wake-On-Lan can only be used with an ATX 2.01 (or above) compliant power supply.

1-6 Power Supply

As with all computer products, a stable power source is necessary for proper and reliable operation. It is even more important for processors that have high CPU clock rates.

The SUPER X5DPA-G/X5DPA-GG accommodates ATX power supplies. Although most power supplies generally meet the specifications required by the CPU, some are inadequate. You should use one that will supply at least 350W of power and includes the additional +12V, 8-pin power connector - an even higher wattage power supply is recommended for high-load configurations. Also your power supply must supply 1.5A for LAN1 and LAN2.

(*NOTES:
Auxiliary 12v power (J15) is necessary to support Intel Xeon CPUs. Failure to provide this extra power will result in the CPUs becoming unstable after only a few minutes of operation. See Section 2-5 for details on connecting the power supply cables.

It is strongly recommended that you use a high quality power supply that meets ATX power supply Specification 2.02 or above. It must also be SSI compliant (info at http://www.ssiforum.org/). Additionally, in areas where noisy power transmission is present, you may choose to install a line filter to shield the computer from noise. It is recommended that you also install a power surge protector to help avoid problems caused by power surges.

1-7 Super I/O

The disk drive adapter functions of the Super I/O chip include a floppy disk drive controller that is compatible with industry standard 82077/765, a data separator, write pre-compensation circuitry, decode logic, data rate selection, a clock generator, drive interface control logic and interrupt and DMA logic. The wide range of functions integrated onto the Super I/O greatly reduces the number of components required for interfacing with floppy disk

drives. The Super I/O supports 360 K, 720 K, 1.2 M, 1.44 M or 2.88 M disk drives and data transfer rates of 250 Kb/s, 500 Kb/s or 1 Mb/s.It also provides two high-speed, 16550 compatible serial communication ports

(UARTs), one of which supports serial infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability and a processor interrupt system.
Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability and a processor interrupt system. Both UARTs provide legacy speed with baud rate of up to 115.2 Kbps as well as an advanced speed with baud rates of 250 K, 500 K, or 1 Mb/s, which support higher speed modems.

The Super I/O supports one PC-compatible printer port (SPP), Bi-directional Printer Port (BPP) , Enhanced Parallel Port (EPP) or Extended Capabilities Port (ECP).

The Super I/O provides functions that comply with ACPI (Advanced Configuration and Power Interface), which includes support of legacy and ACPI power management through an SMI or SCI function pin. It also features auto power management to reduce power consumption.

The IRQs, DMAs and I/O space resources of the Super I/O can flexibly adjust to meet ISA PnP requirements, which support ACPI and APM (Advanced Power Management).

Chapter 2
Installation

2-1 Static-Sensitive Devices

Electric-Static-Discharge (ESD) can damage electronic components. To prevent damage to your system board, it is important to handle it very carefully. The following measures are generally sufficient to protect your equipment from ESD.

Precautions

- Use a grounded wrist strap designed to prevent static discharge.
- Touch a grounded metal object before removing the board from the antistatic bag.
- Handle the board by its edges only; do not touch its components, peripheral chips, memory modules or gold contacts.
- When handling chips or modules, avoid touching their pins.
- Put the motherboard and peripherals back into their antistatic bags when not in use.
- For grounding purposes, make sure your computer chassis provides excellent conductivity between the power supply, the case, the mounting fasteners and the motherboard.

Unpacking

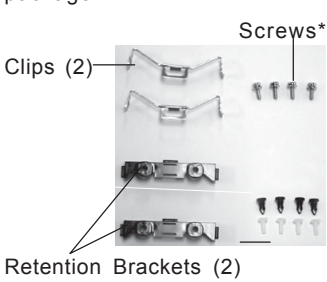
The motherboard is shipped in antistatic packaging to avoid static damage. When unpacking the board, make sure the person handling it is static protected.

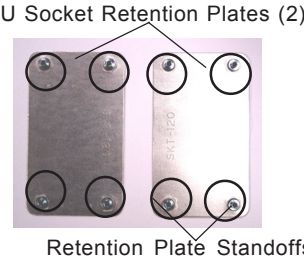
2-2 PGA Processor and Heatsink Installation

When handling the processor package, avoid placing direct pressure on the label area of the fan. Also, do not place the motherboard on a conductive surface, which can damage the BIOS battery and prevent the system from booting up.

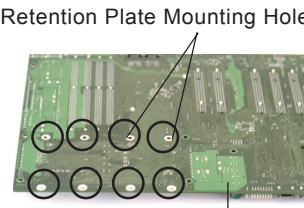
IMPORTANT: Always connect the power cord last and always remove it before adding, removing or changing any hardware components. Make sure that you install the processor into the CPU socket **before** you install the CPU heat sink.

1. Locate the following components, which are included in the shipping package.



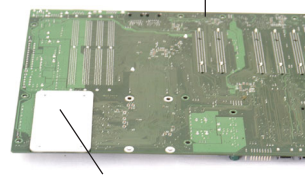


2. On the back side of the motherboard, locate the four CPU Retention Plate mounting holes. Also, Locate the four standoffs on each of the Retention Plates (shown on the pictures on the right).



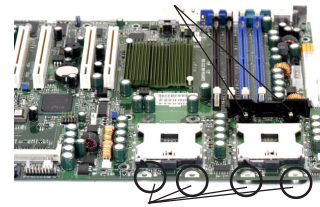
3. Make sure that the small sheet of Mylar is attached on the surface of the Retention Plate. Align the standoffs of the Retention Plate with the four mounting holes on the motherboard.

4. Place the Retention Plate on the back side of the motherboard and lock it into the proper position by inserting the standoffs on the Retention Plate into the mounting holes on the motherboard (with the Mylar sheet in between).

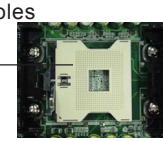


5. On the front side of the motherboard, place a Retention Bracket on top of the CPU socket. Make sure to

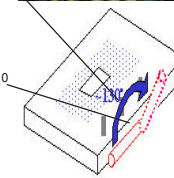
line up the mounting holes on the bracket against the mounting holes on the motherboard. Secure the Retention Bracket (on the front) and the Retention Plate (on the back) by putting screws through the mounting holes. Repeat this step for the second Retention Bracket.



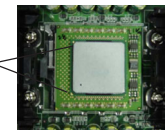
6. Repeat Steps 2-5 to install the additional CPU Retention Plate and the Retention Brackets.



7. Lift the lever on the CPU socket: *lift the lever completely and fully (*120º to 135º for Xeon CPUs as shown on right), or you will damage the CPU socket when power is applied. (Install CPU1 first.)*

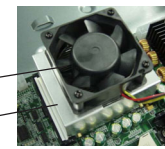


8. Install the CPU in the socket. Make sure that pin 1 of the CPU is seated on pin 1 of the socket (both corners are marked). When using only one CPU, install it into CPU socket #1 (CPU socket #2 is automatically disabled if only one CPU is used).

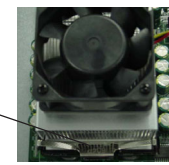


9. Press the lever down until you hear it *click* into the locked position.

10. Apply the proper amount of thermal glue to the CPU die and place the heatsink and fan on top of the CPU.

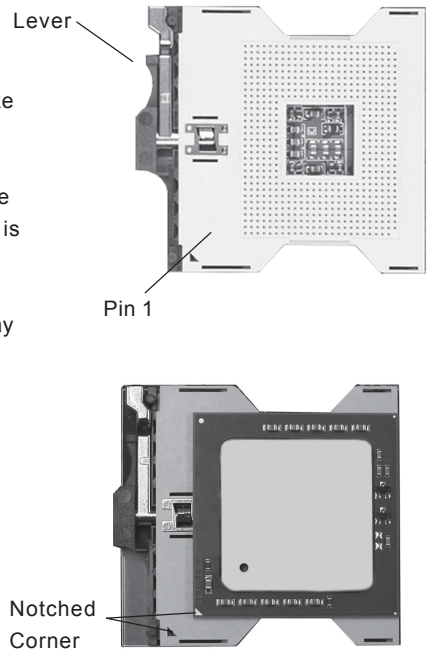


11. Secure the heatsink by locking the retention clips into their proper position.



12. Connect the three wires of the CPU fan to the respective CPU fan connector.

Figure 2-1. PGA604 Socket: Empty and with Processor Installed



Warning! Make sure you lift the lever completely when installing the CPU. If the lever is only partly raised, damage to the socket or CPU may result.

Mounting the Motherboard in the Chassis

All motherboards have standard mounting holes to fit different types of chassis. Make sure the location of all the mounting holes for both the motherboard and the chassis match. Although a chassis may have both plastic and metal mounting fasteners, metal ones are highly recommended because they ground the motherboard to the chassis. Make sure the metal standoffs click in or are screwed in tightly. Then use a screwdriver to secure the motherboard onto the motherboard tray.

2-3 Installing DIMMs

Note: Check the Supermicro web site for recommended memory modules: http://www.supermicro.com/TECHSUPPORT/FAQs/Memory_vendors.htm

CAUTION

Exercise extreme care when installing or removing DIMM modules to prevent any possible damage. Also note that the memory is interleaved to improve performance (see step 1).

DIMM Installation (See Figure 2-2)

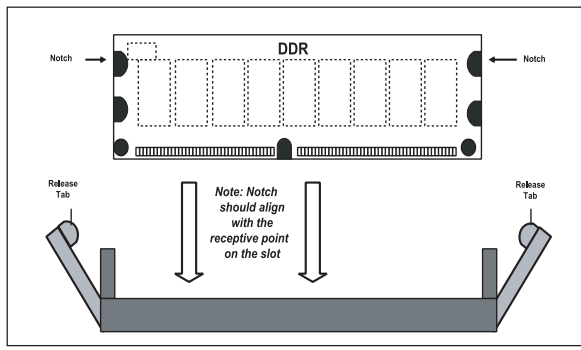
1. Insert the desired number of DIMMs into the memory slots, starting with Bank 1. The memory scheme is interleaved so you must install two modules at a time, beginning with Bank 1, then Bank 2.
2. Insert each DIMM module vertically into its slot. Pay attention to the notch along the bottom of the module to prevent inserting the DIMM module incorrectly.
3. Gently press down on the DIMM module until it snaps into place in the slot. Repeat for all modules (see step 1 above).

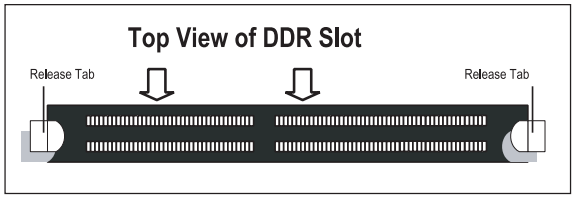
Memory Support

The X5DPA-G/X5DPA-GG only supports ECC registered DDR-266/200 MHz SDRAM memory. If you are using 533 MHz front side bus processor(s), you must use DDR-266 SDRAM. If you are using 400 MHz front side bus processor(s), you may use either DDR-266 or DDR-200 SDRAM.

Figure 2-2. Installing and Removing DIMMs

To Install: Insert module vertically and press down until it snaps into place. Pay attention to the alignment notch at the bottom.



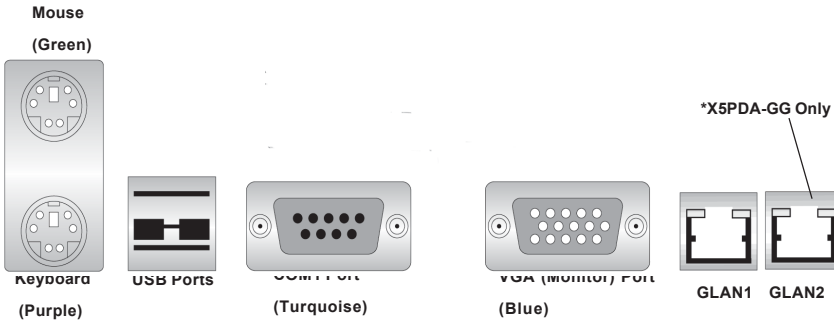


To Remove:
Use your thumbs to gently push near the edge of both ends of the module. This should release it from the slot.

2-4 I/OPorts/Control Panel Connectors

The I/O ports are color coded in conformance with the PC 99 specification. See Figure 2-3 below for the colors and locations of the various I/O ports.

Figure 2-3. I/O Port Locations and Definitions



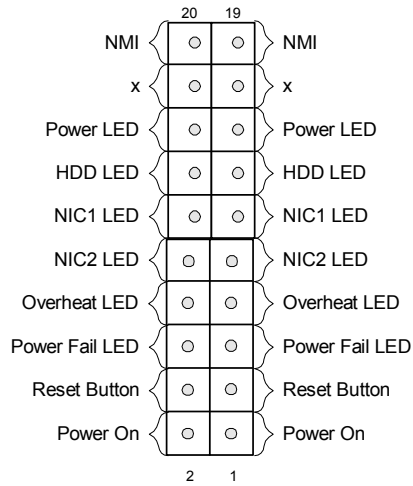
X5DPA-G(GLAN1 Only)/X5DPA-GG(GLAN1 & GLAN2)

Notes: COM2 is a header located on the motherboard - see the motherboard layout pages in Chapter 1 for location.

Front Control Panel

JF2 contains header pins for various buttons and indicators that are normally located on a control panel at the front of the chassis. These connectors are designed specifically for use with Supermicro server chassis. See Figure 2-4 for the descriptions of the various control panel buttons and LED indicators. Refer to the following section for descriptions and pin definitions.

Figure 2-4. JF2 Header Pins



2-5 Connecting Cables

ATX Power Connection

The X5DPA-G/X5DPA-GG power supply connector meets the SSI (Superset ATX) 24-pin specification, however it also supports a 20-pin power supply connector. Make sure that the orientation of the PS connector is correct. The X5DPA-G/X5DPA-GG has the 24-pin connector. See the tables on the right for pin definitions.

ATX Power Supply 24-pin Connector Pin Definitions

Pin Number	Definition	Pin Number	Definition
13	+3.3V	1	+3.3V
14	-12V	2	+3.3V
15	COM	3	COM
16	PS_ON#	4	+5V
17	COM	5	COM
18	COM	6	+5V
19	COM	7	COM
20	Res(NC)	8	PWR_OK
21	+5V	9	5VSB
22	+5V	10	+12V
23	+5V	11	+12V
24	COM	12	+3.3V

PWR_SEC Connection

In addition to the Primary ATX power connector (above), the Secondary 12v 8-pin J15 connector must also be connected to your power supply. See the table on the right for pin definitions.

8-Pin +12v Power Supply Connector (J15)

Pins	Definition
1 thru 4	Ground
5 thru 8	+12v

Power LED

The Power LED connection is located on pins 15 and 16 of JF2. Refer to the table on the right for pin definitions.

PWR_LED Pin Definitions (JF2)

Pin Number	Definition
15	Vcc
16	Control

NMI Button

The non-maskable interrupt button header is located on pins 19 and 20 of JF2. Refer to the table on the right for pin definitions.

NMI Button Pin Definitions (JF2)

Pin Number	Definition
19	Control
20	Ground

HDD LED

The HDD LED (for IDE and SCSI Disk Drives) connection is located on pins 13 and 14 of JF2. Attach the IDE hard drive LED cable to these pins to display disk activity. Refer to the table on the right for pin definitions.

HDD LED Pin Definitions (JF2)

Pin Number	Definition
13	Vcc
14	HD Active

NIC1 LED

The NIC1 (Network Interface Controller) LED connection is located on pins 11 and 12 of JF2. Attach the NIC1 LED cable to display network activity. Refer to the table on the right for pin definitions.

NIC1 LED Pin Definitions (JF2)

Pin Number	Definition
11	Vcc
12	GND

NIC2 LED (*X5DPA-GG Only)

The NIC2 (Network Interface Controller) LED connection is located on pins 9 and 10 of JF2. Attach the NIC2 LED cable to display network activity. Refer to the table on the right for pin definitions.

NIC2 LED Pin Definitions (JF2)

Pin Number	Definition
9	Vcc
10	GND

Overheat LED (OH)

Connect an LED to the OH connection on pins 7 and 8 of JF2 to provide advanced warning of chassis overheating. Refer to the table on the right for pin definitions.

Overheat (OH) LED Pin Definitions (JF2)

Pin Number	Definition
7	Vcc
8	GND

Power Fail LED

The Power Fail LED connection is located on pins 5 and 6 of JF2. Refer to the table on the right for pin definitions.

Power Fail LED Pin Definitions (JF2)

Pin Number	Definition
5	Vcc
6	GND

Reset Button

The Reset Button connection is located on pins 3 and 4 of JF2. Attach it to the hardware reset switch on the computer case. Refer to the table on the right for pin definitions.

Reset Pin Definitions (JF2)

Pin Number	Definition
3	Reset
4	Ground

Power Button

The Power Button connection is located on pins 1 and 2 of JF2. Momentarily contacting both pins will power on/off the system. This button can also be configured to function as a suspend button (see the Power Button Mode setting in BIOS). To turn off the power when set to suspend mode, depress the button for at least 4 seconds. Refer to the table on the right for pin definitions.

Power Button Connector Pin Definitions (JF2)

Pin Number	Definition
1	PW_ON
2	Ground

Chassis Intrusion

A Chassis Intrusion header is located at JL1. Attach the appropriate cable to inform you of a chassis intrusion.

Back Panel Universal Serial Bus (USB0/1)

Two Universal Serial Bus ports (J10, J11) are located beside the PS/2 keyboard/mouse ports. USB0 is the bottom connector and USB1 is the top connector. See the table on the right for pin definitions.

Back Panal Universal Serial Bus Pin Definitions (J10, J11)

USB0		USB1	
Pin Number	Definition	Pin Number	Definition
1	+5V	1	+5V
2	P0-	2	P0-
3	P0+	3	P0+
4	Ground	4	Ground

Front Panel USB 0/1 & USB 2

Three Front Panel USB Headers (JD2, J22) can be used for front side USB access. These USB headers are located next to the Floppy Disk Connector. You will need a USB cable (not included) to use either connection. Refer to the tables on the right for pin definitions.

Front Panel Universal Serial Bus Pin Definitions

USB0/1(JD2)		USB2(J22)	
Pin Number	Definition	Pin Number	Definition
1	+5V	1	+5V
2	P0-	2	P0-
3	P0+	3	P0+
4	Ground	4	Ground
5	Key	5	N/A

Serial Ports

The COM1(J8) serial port is located next to the USB 0/1 ports. COM 2 is located at the corner near PCI-33 Slots. (see MB layouts in Chapter 1). See the table on the right for pin definitions. The COM2(J26) connector is a header on the motherboard (see pp. 1-6, 1-8 for location).

Serial Port Pin Definitions (COM1, COM2)

Pin Number	Definition	Pin Number	Definition
1	CD	6	DSR
2	RD	7	RTS
3	TD	8	CTS
4	DTR	9	RI
5	Ground	10	NC

Note: Pin 10 is included on the header but not on the port.

Ethernet Ports GLAN1/2

(*GLAN 2 is for X5DPA-GG Only)

Two Ethernet ports (designated GLAN1 and GLAN2) are located beside the VGA port on the IO backplane. These ports accept RJ45 type cables.

Fan Headers

The X5DPA-G/X5DPA-GG has five CPU, chassis fan headers. Designations include CPU Fan1, CPU Fan2, Chassis Fan 3, Chassis Fan4, and Chassis Fan 5. See the table on the right for pin definitions.

Fan Header Pin Definitions

Pin Number	Definition
1	Ground (black)
2	+12V (red)
3	Tachometer

Caution: These fan headers are DC power.

Power LED/Speaker/NMI

On the JD1 header, pins 1-3 are for a Power LED, pins 4-7 are for the speaker. See the table on the right for speaker pin definitions. Note: The speaker connector pins are for use with an external speaker. If you wish to use the onboard speaker, you should close pins 6-7 with a jumper.

Speaker Connector Pin Definitions (JD1)

Pin Number	Function	Definition
4	+	Red wire, Speaker data
5	Key	No connection
6		Key
7		Speaker data

ATX PS/2 Keyboard and PS/2 Mouse Ports

The ATX PS/2 keyboard and PS/2 mouse are located on J28 on the X5DPA-G/X5DPA-GG. See the table at right for pin definitions. (See Figure 2-3 for the locations of each.)

PS/2 Keyboard and Mouse Port Pin Definitions (J28)

Pin Number	Definition
1	Data
2	NC
3	Ground
4	VCC
5	Clock
6	NC

Wake-On-LAN

The Wake-On-LAN header is designated WOL1. See the table on the right for pin definitions. You must enable the LAN Wake-Up setting in BIOS to use this feature. You must also have a LAN card with a Wake-on-LAN connector and cable.

Wake-On-LAN Pin Definitions (WOL1)

Pin Number	Definition
1	+5V Standby
2	Ground
3	Wake-up

Wake-On-Ring

The Wake-On-Ring header is designated JWOR1. This function allows your computer to receive and "wake-up" by an incoming call to the modem when in suspend state. See the table on the right for pin definitions. You must have a Wake-On-Ring card and cable to use this feature.

Wake-on-Ring Pin Definitions (JWOR1)

Pin Number	Definition
1	Ground
2	Wake-up

Keylock

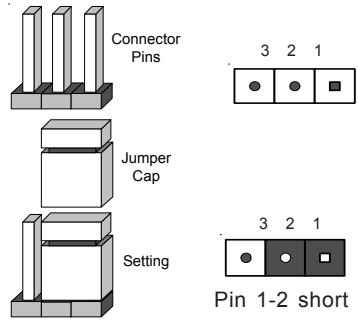
The keyboard lock connection is located on JP35. Utilizing this header allows you to inhibit any actions made on the keyboard, effectively "locking" it.

2-6 Jumper Settings

Explanation of Jumpers

To modify the operation of the motherboard, jumpers can be used to choose between optional settings. Jumpers create shorts between two pins to change the function of the connector. Pin 1 is identified with a square solder pad on the printed circuit board. See the motherboard layout pages for jumper locations.

Note: On two pin jumpers, "Closed" means the jumper is on and "Open" means the jumper is off the pins.



CMOS Clear

JBT1 is not literally a jumper but consists of two contact pads. To clear the contents of CMOS, short these pads together by touching them both with a metal conductor such as the head of a small screwdriver. For ATX power supplies, you must completely shut down the system and remove the AC power cord before clearing CMOS.

GLAN Enable/Disable

(*GLAN2 is for X5DPA-GG only)

Change the setting of JP3 to enable or disable the onboard GLAN1. Change the setting of JP6 to enable or disable the onboard GLAN2 (*X5DPA-GG only). See the table on the right for jumper settings. The default setting is enabled

LAN Enable/Disable Jumper Settings (JP3: LAN 1, JP6: LAN2)

Jumper Position	Definition
Pins 1-2	Enabled
Pins 2-3	Disabled

VGA Enable/Disable

JP4 allows you to enable or disable the VGA port. The default position is on pins 1 and 2 to enable VGA. See the table on the right for jumper settings.

VGA Enable/Disable Jumper Settings (JP4)

Jumper Position	Definition
1-2	Enabled
2-3	Disabled

Front Side Bus Speed

JP39 (see motherboard layout) is used to set the system (front side) bus speed for the processors. It is best to keep this jumper set to Auto. This jumper is used together with the CPU Clock setting in BIOS. See the table on the right for jumper settings.

Front Side Bus Speed Jumper Settings (JP39)

Jumper Position	Definition
Pins 1-2	Auto
Pins 2-3	400 MHz
Open	533 MHz

Watch Dog Enable/Disable

JP37 allows you to enable or disable the functions of Watch Dog. See the table on the right for jumper settings. Close Pins 1-2 for reset. Close Pins 2-3 to activate the function of NMI (Non Maskable Interrupt).

Watch Dog Enable/ Disable Jumper Settings (JP37)

Jumper Position	Definition
1-2	Reset
2-3	NMI

2-7 Onboard Indicators

GLAN1/GLAN2 LEDs (GLAN2 is for X5DPA-GG Only)

The Ethernet ports (located beside the VGA port) have two LEDs. See the table on the right for the functions associated with these LEDs. On each GLAN port, the yellow LED indicates activity while the other LED may be green, orange or off to indicate the speed of the connection.

GLAN Right LED Indicator

LED Color	Definition
Off	No Connection
Green	100 MHz
Orange	1 GHz

2-8 Floppy/Hard Disk Drive, Parallel Port, and IPMI Connections (*Parallel Port: X5DPA-G, IPMI: X5DPA-GG)

Note the following when connecting the floppy and hard disk drive cables:

- The floppy disk drive cable has seven twisted wires.
- A red mark on a wire typically designates the location of pin 1.
- A single floppy disk drive ribbon cable has 34 wires and two connectors to provide for two floppy disk drives. The connector with twisted wires always connects to drive A, and the connector that does not have twisted wires always connects to drive B.

Parallel Port Connector (*X5PDA-G only)

J7 is designated as the parallel (printer) port connector for the X5DPA-G motherboard. See the table on the right for pin definitions.

Parallel (Printer) Port Pin Definitions (J7)

Pin Number	Function	Pin Number	Function
1	Strobe-	2	Auto Feed-
3	Data Bit 0	4	Error-
5	Data Bit 1	6	Init-
7	Data Bit 2	8	SLCT IN-
9	Data Bit 3	10	GND
11	Data Bit 4	12	GND
13	Data Bit 5	14	GND
15	Data Bit 6	16	GND
17	Data Bit 7	18	GND
19	ACK	20	GND
21	BUSY	22	GND
23	PE	24	GND
25	SLCT	26	NC

IPMI (*X5PDA-GG only)

J22 is designated as the IPMI Socket for the X5DPA-GG Motherboard.

Floppy Connector

The floppy connector is located on JP7. See the table below for pin definitions.

Floppy Connector Pin Definitions (JP7)

Pin Number	Function	Pin Number	Function
1	GND	2	FDHDIN
3	GND	4	Reserved
5	Key	6	FDEDIN
7	GND	8	Index-
9	GND	10	Motor Enable
11	GND	12	Drive Select B-
13	GND	14	Drive Select A-
15	GND	16	Motor Enable
17	GND	18	DIR-
19	GND	20	STEP-
21	GND	22	Write Data-
23	GND	24	Write Gate-
25	GND	26	Track 00-
27	GND	28	Write Protect-
29	GND	30	Read Data-
31	GND	32	Side 1 Select-
33	GND	34	Diskette

IDE Connectors

There are no jumpers to configure the onboard IDE#1(J2) and IDE#2 (J3) connectors. See the table on the right for pin definitions.

IDE Connector Pin Definitions (IDE#1, IDE#2)

Pin Number	Function	Pin Number	Function
1	Reset IDE	2	GND
3	Host Data 7	4	Host Data 8
5	Host Data 6	6	Host Data 9
7	Host Data 5	8	Host Data 10
9	Host Data 4	10	Host Data 11
11	Host Data 3	12	Host Data 12
13	Host Data 2	14	Host Data 13
15	Host Data 1	16	Host Data 14
17	Host Data 0	18	Host Data 15
19	GND	20	Key
21	DRQ3	22	GND
23	I/O Write-	24	GND
25	I/O Read-	26	GND
27	IOCHRDY	28	BALE
29	DACK3-	30	GND
31	IRQ14	32	IOCS16-
33	Addr 1	34	GND
35	Addr 0	36	Addr 2
37	Chip Select 0	38	Chip Select 1-
39	Activity	40	GND

2-9 Installing Software Drivers

After all the hardware has been installed, you must install the software drivers. The necessary drivers are all included on the Supermicro CD that came packaged with your motherboard. After inserting this CD into your CDROM drive, the display shown in Figure 2-5 should appear. (If this display does not appear, click on the My Computer icon and then on the icon representing your CDROM drive. Finally, double click on the S "Setup" icon.)

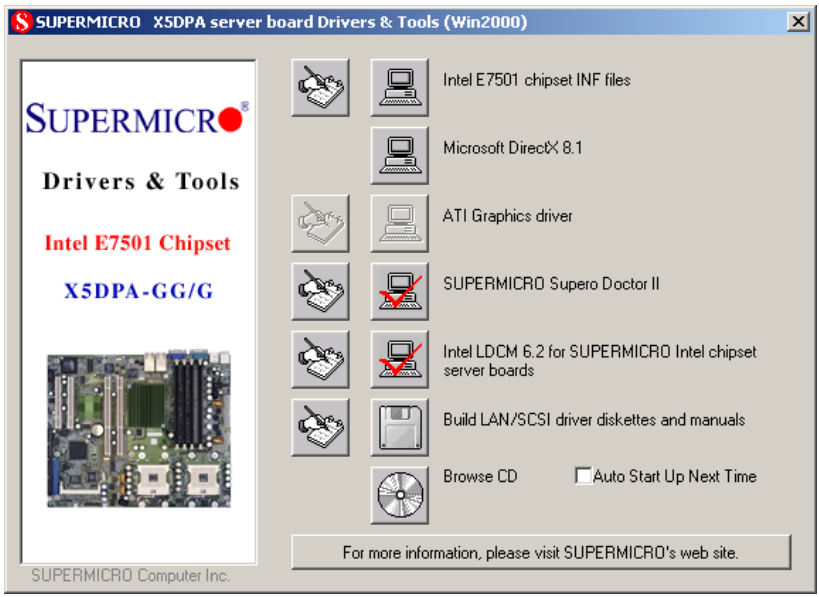


Figure 2-5. Driver/Tool Installation Display Screen

Click the icons showing a hand writing on paper to view the readme files for each item. The bottom icon with a CD on it allows you to view the entire contents of the CD.

Notes

Chapter 3
Troubleshooting

3-1 Troubleshooting Procedures

Use the following procedures to troubleshoot your system. If you have followed all of the procedures below and still need assistance, refer to the 'Technical Support Procedures' and/or 'Returning Merchandise for Service' section(s) in this chapter.

Note: Always disconnect the power cord before adding, changing or installing any hardware components.

Before Power On

1. Make sure no short circuits exist between the motherboard and chassis.
2. Disconnect all ribbon/wire cables from the motherboard, including those for the keyboard and mouse.
3. Remove all add-on cards.
4. Install one CPU (making sure it is fully seated) and connect the chassis speaker and the power LED to the motherboard. (Check all jumper settings as well.)

No Power

1. Make sure no short circuits exist between the motherboard and the chassis.
2. Verify that all jumpers are set to their default positions.
3. Check that the 115V/230V switch on the power supply is properly set.
4. Turn the power switch on and off to test the system.
5. The battery on your motherboard may be old. Check to verify that it still supplies ~3VDC. If it does not, replace it with a new one.

No Video

1. If the power is on but you have no video, remove all the add-on cards and cables.
2. Use the speaker to determine if any beep codes exist. Refer to the Appendix for details on beep codes.

NOTE

If you are a system integrator, VAR or OEM, a POST diagnostics card is recommended. For I/O port 80h codes, refer to App. B.

Memory Errors

1. Make sure the DIMM modules are properly and fully installed.
2. Determine if different speeds of DIMMs have been installed and verify that the BIOS setup is configured for the fastest speed of RAM used. It is recommended to use the same RAM speed for all DIMMs in the system.
3. Make sure you are using registered ECC, DDR-266 or DDR-200 SDRAM. If using 533 MHz processors, you must use DDR-266 memory (DDR-200 is not supported at a 533 MHz front side bus speed).
4. Check for bad DIMM modules or slots by swapping a single module between two slots and noting the results.
5. Make sure all memory modules are fully seated in their slots. As an interleaved memory scheme is used, you must install two modules at a time, beginning with Bank 1, then Bank 2, and so on (see Section 2-3).
6. Check the power supply voltage 115V/230V switch.

Losing the System's Setup Configuration

1. Ensure that you are using a high quality power supply. A poor quality power supply may cause the system to lose the CMOS setup information. Refer to Section 1-6 for details on recommended power supplies.
2. The battery on your motherboard may be old. Check to verify that it still supplies ~3VDC. If it does not, replace it with a new one.
3. If the above steps do not fix the Setup Configuration problem, contact your vendor for repairs.

3-2 Technical Support Procedures

Before contacting Technical Support, please take the following steps. Also, note that as a motherboard manufacturer, Super Micro does not sell directly to end-users, so it is best to first check with your distributor or reseller for troubleshooting services. They should know of any possible problem(s) with the specific system configuration that was sold to you.

1. Please go through the 'Troubleshooting Procedures' and 'Frequently Asked Question' (FAQ) sections in this chapter or see the FAQs on our web site (http://www.supermicro.com/techsupport.htm) before contacting Technical Support.

2. BIOS upgrades can be downloaded from our web site at http://www.supermicro.com/techsupport/download.htm.

Note: Not all BIOS can be flashed depending on the modifications to the boot block code.

3. If you still cannot resolve the problem, include the following information when contacting Super Micro for technical support:
   - Motherboard model and PCB revision number
   - BIOS release date/version (this can be seen on the initial display when your system first boots up)
   - System configuration

   An example of a Technical Support form is on our web site at http://www.supermicro.com/techsupport/contact_support.htm.
4. Distributors: For immediate assistance, please have your account number ready when placing a call to our technical support department. We can be reached by e-mail at support@supermicro.com or by fax at: (408) 503-8000, option 2.

3-3 Frequently Asked Questions

Question: What are the various types of memory that my motherboard can support?

Answer: The X5DPA-G/X5DPA-GG has four DIMM slots that support 184-pin, registered ECC DDR-266 or DDR-200 SDRAM DIMM modules. If using 533 MHz processors, you must use DDR-266 memory (DDR-200 is not supported at a 533 MHz front side bus speed). However, DDR-266 runs at 200 MHz if a 400MHz CPU is used. It is strongly recommended that you do not mix memory modules of different speeds and sizes. Unbuffered SDRAM, non-ECC memory and PC100/133 SDRAM modules are not supported.

Question: How do I update my BIOS?

Answer: It is recommended that you **do not** upgrade your BIOS if you are experiencing no problems with your system. Updated BIOS files are located on our web site at http://www.supermicro.com. Please check our BIOS warning message and the info on how to update your BIOS on our web site. Also, check the current BIOS revision and make sure it is newer than your BIOS before downloading. Select your motherboard model and download the BIOS file to your computer.

Question: What's on the CD that came with my motherboard?

Answer: The supplied compact disc has quite a few drivers and programs that will greatly enhance your system. We recommend that you review the CD and install the applications you need. Applications on the CD include chipset drivers for Windows and security and audio drivers.

Question: Why can't I turn off the power using the momentary power on/off switch?

Answer: The instant power off function is controlled in BIOS by the Power Button Mode setting. When the On/Off feature is enabled, the motherboard will have instant off capabilities as long as the BIOS has control of the system. When the Standby or Suspend feature is enabled or when the BIOS is not in control such as during memory count (the first screen that appears when the system is turned on), the momentary on/off switch must be held for more than four seconds to shut down the system. This feature is required to implement the ACPI features on the motherboard.

3-4 Returning Merchandise for Service

A receipt or copy of your invoice marked with the date of purchase is required before any warranty service will be rendered. You can obtain service by calling your vendor for a Returned Merchandise Authorization (RMA) number. When returning to the manufacturer, the RMA number should be prominently displayed on the outside of the shipping carton, and mailed prepaid or hand-carried. Shipping and handling charges will be applied for all orders that must be mailed when service is complete.

This warranty only covers normal consumer use and does not cover damages incurred in shipping or from failure due to the alternation, misuse, abuse or improper maintenance of products.

During the warranty period, contact your distributor first for any product problems.

Notes

Chapter 4
AMIBIOS

4-1 Introduction

This chapter describes the AMIBIOS for the X5DPA-G/X5DPA-GG. The AMI ROM BIOS is stored in a Flash EEPROM and can be easily upgraded using a floppy disk-based program. This chapter describes the basic navigation of the AMI BIOS Setup Utility setup screens.

Starting BIOS Setup Utility

To enter the AMI BIOS Setup Utility screens, hit the <Delete> key while the system is booting-up.

(*Note: In most cases, the <Delete> key is used to invoke the BIOS setup screen. There are a few cases when other keys are used, such as <F1>, <F2>, and so on.)

Each main BIOS menu option is described in this user's guide. The Main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. "Grayed-out" options cannot be configured. Options in blue can be configured by the user. The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

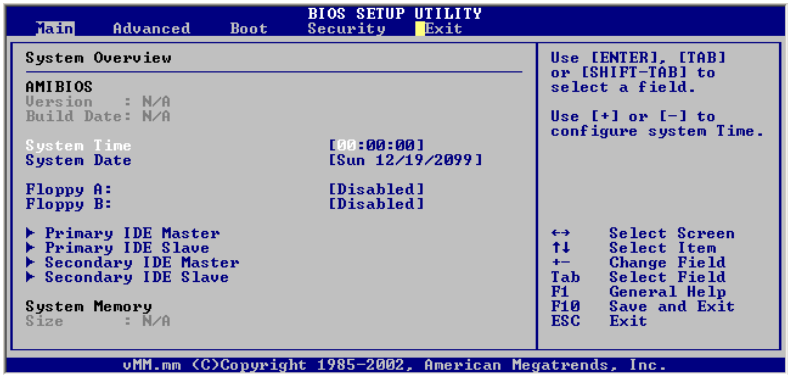
(*Note: AMIBIOS has default text messages built in. Supermicro retains the option to include, omit, or change any of these text messages.)

The AMI BIOS setup/utility uses a key-based navigation system called hot keys. Most of the BIOS setup utility hot keys can be used at any time during the setup navigation process. These keys include <F1>, <F10>, <Enter>, <ESC>, <Arrow> keys, and so on.

(*Note: Options printed in **Bold** are default settings.)

4-2 Main Setup

When you first enter the BIOS Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the ***Main*** tab on the top of the screen. The Main BIOS Setup screen is shown below.



System Time/System Date

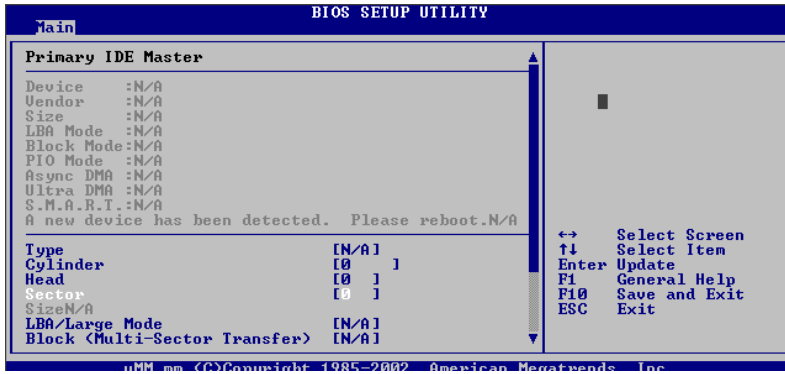
Use this option to change the system time and date. Highlight *System Time* or *System Date* using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

*__Note:__ The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30P.M. as 17:30:00.

Floppy A:/Floppy B:

Move the cursor to these fields via up and down <arrow> keys. Select the floppy type. The options are "Disabled", "360 KB 51/4", "1.2 MB 51/4"," 720 KB 31/2", **"1.44 MB 3½"**, and **"2.88 MB 3½"**.

▶Primary IDE Master/Slave, Secondary IDE Master/Slave Sub Menu



▶Primary and Secondary IDE Master and Slave Settings

From the Main Setup screen, press <Enter> to access the sub menu for the primary and secondary IDE master and slave drives. Use this screen to select options for the Primary and Secondary IDE drives. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. The settings are described on the following pages. The screen for the Primary IDE Master is shown below.

Type

Select the type of device connected to the system. The options are "Not Installed", "**Auto**", "CDROM" and "ARMD".

Cylinder/Header/Sector

These features allow the BIOS to auto-detect and display the status of Cylinder/Header/Sector.

LBA/Large Mode

LBA (Logical Block Addressing) is a method of addressing data on a disk drive. In LBA mode, the maximum drive capacity is 137 GB. For drive capacities over 137 GB, your system must be equipped with 48-bit LBA mode addressing. If not, contact your manufacturer or install an ATA/133 IDE controller card that supports 48-bit LBA mode. The options are "Disabled" or "**Auto**".

Block (Multi-Sector Transfer)

Block mode boosts IDE drive performance by increasing the amount of data transferred. Only 512 bytes of data can be transferred per interrupt if block mode is not used. Block mode allows transfers of up to 64 KB per interrupt. Select "Disabled" to allow the data to be transferred from and to the device one sector at a time. Select "Auto" to allows the data transfer from and to the device occur multiple sectors at a time if the device supports it. The options are "**Auto**" and "Disabled".

PIO Mode

IDE PIO (Programmable I/O) mode programs timing cycles between the IDE drive and the programmable IDE controller. As the PIO mode increases, the cycle time decreases. The options are "**Auto**", "0", "1", "2", "3", and "4". Select Auto to allow the BIOS to auto detect the PIO mode. Use this value if the IDE disk drive support cannot be determined. Select 0 to allow the BIOS to use PIO mode 0. It has a data transfer rate of 3.3 MBs. Select 1 to allow the BIOS to use PIO mode 1. It has a data transfer rate of 5.2 MBs. Select 2 to allow the BIOS to use PIO mode 2. It has a data transfer rate of 8.3 MBs. Select 3 to allow the BIOS to use PIO mode 3. It has a data transfer rate of 11.1 MBs. Select 4 to allow the BIOS to use PIO mode 4. It has a data transfer rate of 16.6 MBs. This setting generally works with all hard disk drives manufactured after 1999. For other disk drives, such as IDE CD-ROM drives, check the specifications of the drive.

DMA Mode

Select Auto to allow the BIOS to auto detect the DMA mode. Use this value if the IDE disk drive support cannot be determined. Select SWDMA0 to allow the BIOS to use Single Word DMA mode 0. It has a data transfer rate of 2.1 MBs. Select SWDMA1 to allow the BIOS to use Single Word DMA mode 1. It has a data transfer rate of 4.2 MBs. Select SWDMA2 to allow the BIOS to use Single Word DMA mode 2. It has a data transfer rate of 8.3 MBs. Select MWDMA0 to allow the BIOS to use Multi Word DMA mode 0. It has a data transfer rate of 4.2 MBs. Select MWDMA1 to allow the BIOS to use Multi Word DMA mode 1. It has a data transfer rate of 13.3 MBs. Select MWDMA2 to allow the BIOS to use Multi-Word DMA mode 2. It has a data transfer rate of 16.6 MBs. Select UDMA0 to allow the BIOS to use Ultra DMA mode 0. It has a data transfer rate of 16.6 MBs. It has the same transfer rate as PIO mode 4 and Multi Word DMA mode 2.

Select UDMA1 to allow the BIOS to use Ultra DMA mode 1. It has a data transfer rate of 25 MBs. Select UDMA2 to allow the BIOS to use Ultra DMA mode 2. It has a data transfer rate of 33.3 MBs. The Options are "**Auto**", "SWDMA0", "SWDMA1", "SWDMA2", "MWDMA0", "MWDMA1", "MWDMA2","UDMA0", "UDMA1", and "UDMA2".

S.M.A.R.T. For Hard disk drives

Self-Monitoring Analysis and Reporting Technology (SMART) can help predict impending drive failures. Select "Auto" to allow BIOS to auto detect hard disk drive support. Select "Disabled" to prevent the BIOS from using the S.M.A.R.T. Select "Enabled" to allow the BIOS to use the S.M.A.R.T. to support hard drive disk. The options are "Disabled", "Enabled", and "**Auto**."

32Bit Data Transfer

Select "Enabled" to activate the function of 32-Bit data transfer. Select "Disabled" to deactivate the function. The options are "Enabled" and "**Disabled**".

ARMD Emulation Type

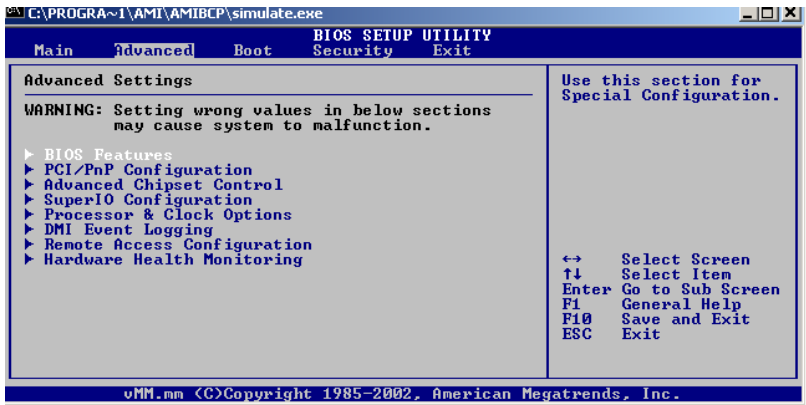
The feature allows the BIOS to set ARMD Emulation type.

System Memory

When AMI BIOS auto detects the System Memory, it will automatically display the size of the memory.

4-3 Advanced BIOS Setup

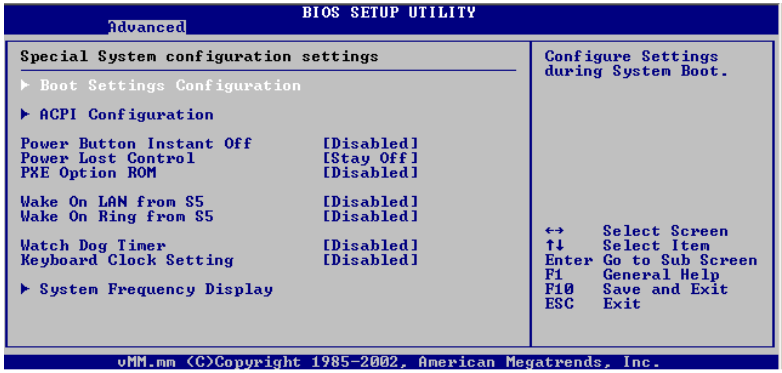
The Advanced BIOS Setup screen is shown below. The sub menus are described on the following pages.



▶BIOS Features

▶Boot Settings Configuration

This item allows the user to configure the system's boot settings.



Quick Boot

The default setting is **"Enabled"**. Select "Disabled" to allow the BIOS to perform all POST tests. Select "Enabled to allow the BIOS to skip certain POST tests to reduce the time needed for the system to boot up.

Quiet Boot

Set this value to allow the boot up screen options to be modified between POST messages or OEM logo. The default setting is **Enabled**. Select Disabled to allow the computer system to display the POST messages. Select Enabled to allow the computer system to display the OEM logo.

Add-On ROM Display Mode

Set this option to display add-on ROM (read-only memory) messages. The default setting is **Force BIOS**. Select "Force BIOS" to allow the computer system to force a third party BIOS to display during system boot. Select "Keep Current" to allow the computer system to display the BIOS information during system boot. The options are "Force BIOS" and "Keep Current".

Boot up Num-Lock

Set this value to allow the Number Lock setting to be modified during boot up. The default setting is **"On**.*"* The options are "On" and "Off".

PS/2 Mouse Support

Set this value to allow the PS/2 mouse support to be modified. The default setting is **Enabled.** The options are "Enabled" and "Disabled".

Wait for 'F1' If Error

Select Enable to activate the function of Wait for "F1" if Error. The options are "**Enabled**" and "Disabled".

Hit 'DEL' Message Display

Select "Enabled" to display Setup Message when the user hits the DEL key. The options are "**Enabled**" and "Disabled".

Interrupt 19 Capture

Select "Enabled" to allow ROMs to trap Interrupt 19. The options are "Enabled" and "**Disabled**."

▶APCI Configuration

This item allows the user to enable or disable ACPI support for the operating system.

ACPI Aware O/S

Select "Yes" if the operating system supports ACPI. Select "No" if the operating system does not support ACPI. The options are "No" and "**Yes**."

▶Advanced APCI Configuration

ACPI 2.0 Features

Select "Yes" to allow RSDP pointers to point to the 64-bit Fixed System Description Tables. Select "No" to deactivate this function. The options are "Yes" and "**No**."

ACPI APIC Support

Select "Enabled" to allow the ACPI APIC Table Pointer to be included in the RSDP pointer list. The options are "**Enabled**", and "Disabled".

AMI OEMB Table

Select "Enabled" to allow the OEMB Table Pointer to be included in the R(x)SDT pointer lists. The options are "**Enabled**", and "Disabled".

Headless Mode

Select "Enabled" to activate the Headless Operation Mode through ACPI. The options are "Enabled", and "**Disabled**".

Power Button Instant Off

Select "Enabled" to activate the function of "Power Button Instant off". The options are "**Enabled**", and "Disabled".

Power Lost Control

Select "Stay Off" if you want the system to remain off when the power recovers from an outage. Select "Power On" if you want the system to be automatically turned on when the power recovers from an outage.
Select "Last State" if you want to system to resume its last state when the power recovers from an outage. The options are "Stay Off", " Power On" and "**Last State**".

PXE Option ROM

Use this feature to enable or disable the function of PXE Option ROM.
The default setting is "**Disabled**."

Wake On LAN from S5

Select "Enabled" to allow the BIOS to Wake Up LAN from S5. The options are "**Enabled**", and "Disabled".

Wake On Ring from S5

Select "Enabled" to activate the function of "Wake On Ring from S5". The options are "**Enabled**", and "Disabled".

Watch Dog Timer

Select "Enabled" to activate Watch Dog Timer. The options are "**Enabled**" or "Disabled".

Keyboard Clock Setting

This feature allows the user to enable or disable the function of Keyboard Clock Setting. The options are: "Enabled" and "Disabled."

▶System Frequency Display

This feature allows the BIOS to display the status, and the frequency of Front Side Bus, Memory and PCI slots.

▶PCI/PnP Configuration

Plug & Play O/S

Select "Yes" to allow the operating system to configure Plug & Play devices that are not required when booting up the system, if the function of Plug & Play is supported by the OS. Select "No" to allow the BIOS to configure Plug & Play devices when the system is booting up. The options are "Yes", and "**No**".

PCI Latency Timer

This option sets the latency of all PCI devices on the PCI bus. The default setting is "64." Select "32" to set the PCI latency to 32 PCI clock cycles. Select "64" to set the PCI latency to 64 PCI clock cycles. Select "96" to set the PCI latency to 96 PCI clock cycles. Select "128" to set the PCI latency to 128 PCI clock cycles. Select "160" to set the PCI latency to 160 PCI clock cycles. Select "192" to set the PCI latency to 192 PCI clock cycles. Select "224" to set the PCI latency to 224 PCI clock cycles. Select "248" to set the PCI latency to 248 PCI clock cycles.

Allocate IRQ to PCI VGA

Set this value to allow or restrict the system from giving the VGA adapter card an interrupt address. The options are "**Yes**" and "No".

Palette Snooping

Set this value to allow the system to modify the Palette Snooping settings. The default setting is "Disabled". This setting should not be changed unless the VGA card manufacturer indicates otherwise. Select "Enabled" to inform the PCI devices that an ISA based Graphics device is installed in the system so that the ISA based Graphics card will function correctly. Always check with your adapter card's manuals first, before modifying the default settings in the BIOS. The options are "Enabled" and "**Disabled**."

PCI IDE BusMaster

Set this value to allow or prevent the use of PCI IDE busmastering. Select "Enabled" to allow the BIOS to use PCI busmaster for reading and writing to IDE drives. The options are "**Disabled**" and "Enabled".

OffBoard PCI/ISA IDE Card

Set this value to allow the OffBoard PCI/ISA IDE Card to be selected. Select "Auto" to allow the BIOS to automatically select the location of an OffBoard PCI IDE adapter card. Select "PCI Slot1" only when there is an IDE adapter card installed in PCI Slot 1. Select "PCI Slot2" only when there is an IDE adapter card installed in PCI Slot 2. Select "PCI Slot 3" only when there is an IDE adapter card installed in PCI Slot 3. Select "PCI Slot 4" only if there is an IDE adapter card installed in PCI Slot 4. The default setting is "Auto".

IRQ

Set this value to allow the IRQ settings to be modified. The default setting is *"***Available***"*. Select "Available" to allow the specified IRQ to be used by a PCI/PnP device. The options are "**Available**" and "Reserved" for the following IRQs. Select "Reserved" to allow the specified IRQ to be used by a legacy ISA device.

IRQ3

IRQ4

IRQ5

IRQ7

IRQ9

IRQ10

IRQ11

IRQ14

IRQ15

DMA

Select "Available" to allow the specified DMA to be used by PCI/PnP device. Select "Reserved" to allow the specified DMA to be used by a legacy ISA device. The options are "**Available**" and "Reserved".

DMA Channel 0

DMA Channel 1

DMA Channel 3

DMA Channel 5

DMA Channel 6

DMA Channel 7

Reserved Memory Size

This item allows the system to reserve memory that is used by ISA devices. Select "Disabled" to prevent BIOS from reserving memory to ISA devices. Select "16K" to allow the system to reserve 16K of the system memory for the ISA devices. Select "32K" to allow the system to reserve 32K of the system memory for the ISA devices. Select "64K" to allow the system for reserve 64K of the system memory to the ISA devices. The default setting is "Disabled".

▶Advanced Chipset Control

▶Intel E7500/7501 NorthBridge Configuration

This feature allows the user to configure the settings for Intel E7500/E7501 NorthBridge chipset.

Chipset Memory Remap Feature

Select "Enabled" to allow remapping of overlapped PCI memory above the total physical memory. The options are "**Enabled**" and "Disabled."

Memory Hole

Select "Enabled" to allow the memory hole to be set from 15M to 16M. The options are "**Disabled**" and "enabled."

▶Intel ICH3 SouthBridge Configuration

This feature allows the user to configure the settings for Intel ICH3 SouthBridge chipset.

ICH3 Dev31 Func1, IDE

Select "Enabled" to enable the ICH3 IDE Controller. The options are "**Enabled**" and "Disabled."

ICH3 Dev31 Func3, SMBUS

Select "Enabled" to enable the ICH3 SMBUS Controller. The options are "**Enabled**" and "Disabled."

ICH3 Dev29 Func0, USB#1

Select "Enabled" to enable the ICH3 USB Host Controller#1. The options are "**Enabled**" and "Disabled."

ICH3 Dev29 Func1, USB#2

Select "Enabled" to enable the ICH3 USB Host Controller#2. The options are "**Disabled**" and "Enabled."

ICH3 Dev29 Func2, USB#3

Select "Enabled" to enable the ICH3 USB Host Controller#3. The options are "**Disabled**" and "Enabled."

ICH3 Positive Decode

Select "Enabled" to activate the function of Positive Decode in ICH3. Select "Enabled" only when the optional Onboard PCI/ISA Bridge is present. The options are "**Disabled**" and "Enabled."

IOAPIC

Select "Enabled" to enable IOAPIC in ICH3. The options are "**Enabled**" and "Disabled."

Extended IOAPIC

Select "Enabled" to enable the extended mode of IOAPIC in ICH3. The options are "**Enabled**" and "Disabled."

CPU B.I.S.T.

Select "Enabled" to enable the function of CPU Built In Self Test. The options are "**Enabled**" and "Disabled."

ICH3 DMA Collection

Select "Enabled" to enable the DMA Collection buffer. The options are "**Enabled**" and "Disabled."

DMA Type

Select the type of DMA performed on this channel. The options are "**LPC DMA**" and "PC/PCI".

DMA-0 Type

DMA-1 Type

DMA-2 Type

DMA-3 Type

DMA-5 Type

DMA-6 Type

DMA-7 Type

▶Intel PCI-64 Hub 2 Configuration

This feature allows the user to configure the settings for Intel PCI-64 Hub2 PCIHub chipset.

HotPlug Inhibit Bus Connect

Select "Enabled" to enable the function of "Inhibit Bus Connect Status" in HotPlug Controller. The options are "**Enabled**" and "Disabled."

PCI Slot1 & Slot2 Frequency

This feature allows the user to set the maximum PCI bus speed to be programmed. When set to "Auto", the bus speed will be decided based on the capabilities of the device on that particular bus. The options are "**Auto**", "33 MHz", "66 MHz", "100 MHz", and "133 MHz".

▶USB Configuration

This feature allows the user to configure USB settings.

Legacy USB Support

Select "Enabled" to enable the support for USB Legacy. The options are "Disabled", and "**Enabled**."

▶USB Mass Storage Device Configuration

This feature allows the user to configure USB Mass Storage Device settings.

USB Mass Storage Reset Delay

This feature allows the user to set the reset delay for USB Mass Storage. The options are "**10 Sec**", "20 Sec", "30 Sec" and "40 Sec".

▶Super IO Configuration

OnBoard Floppy Controller

Select "Enabled" to enable the Onboard Floppy Controller. The options are "Disabled", and "**Enabled**."

Serial Port1 Address

This option specifies the base I/O port address and Interrupt Request address of serial port 1. Select "Disabled" to prevent the serial port from accessing any system resources. When this option is set to *Disabled*, the serial port physically becomes unavailable.

Select "3F8/IRQ4" to allow the serial port to use 3F8 as its I/O port address and IRQ 4 for the interrupt address. The options are "Disabled", "3F8/IRQ4", "3E8/IRQ4", "2E8/IRQ3".

Serial Port2 Address

This option specifies the base I/O port address and Interrupt Request address of serial port 2. Select "Disabled" to prevent the serial port from accessing any system resources. When this option is set to "Disabled", the serial port physically becomes unavailable. Select "2F8/IRQ3" to allow the serial port to use 2F8 as its I/O port address and IRQ 3 for the interrupt address. The options are "Disabled", "2F8/IRQ3", "3E8/IRQ4", "2E8/IRQ3".

Serial Port2 Mode

This feature sets Serial Port2 Mode. The options are "Normal", "IrDA", and "ASK IR". The default setting is "**Normal**".

IR I/O Pin Select

This feature allows the BIOS to select Receiver and Transmitting Pin for Serial Port2. The default setting is "**IR Mode**".

IR Duplex Mode

This feature allows the BIOS to select Full or Half Duplex for Serial Port2. The default setting is "**IR Mode**".

Parallel Port Address

This option specifies the I/O address used by the parallel port. Select "Disabled" to prevent the parallel port from accessing any system resources. When the value of this option is set to "Disabled", the printer port becomes unavailable. Select "378" to allow the parallel port to use 378 as its I/O port address. The majority of parallel ports on computer systems use IRQ7 and I/O Port 378H as the standard setting. Select "278" to allow the parallel port to use 278 as its I/O port address. Select "3BC" to allow the parallel port to use 3BC as its I/O port address. The default setting is "**Disabled**."

Parallel Port Mode

This feature allows BIOS to select Parallel Port Mode. The options are "Normal", "Bi-Directional", "EPP" and "ECP". The default setting is "**Normal**".

Parallel Port IRQ

This feature allows BIOS to select Parallel Port IRQ. The options are "IRQ 5" and "". The default setting is **"IRQ 7"**.

▶Processor & Clock Options

HyperThreading

Select "Enabled" to enabled the function of HyperThreading for HT supported processor(s). The Options are "**Enabled**" or "Disabled."

Ratio CMOS Setting

This feature allows the user to set the ratio between CPU Core Clock and the FSB Frequency. The default setting is "8".

Spread Spectrum

Select "Enabled" to activate the function of "Spread Spectrum" in order to reduce the possibility of Electromagnetic Interference. The options are "Enabled" and "**Disabled**."

▶DMI Event Logging

View Event Log

Highlight this item and press <Enter> to view the contents of the event log.

Mark All Events as Read

Highlight this item and press <Enter> to mark the DMI events as read.

Clear Event Log

This setting will clear all event logs when set to "OK". Options are "OK" and **"Cancel"**.

Event Log Statistics

This setting allows you to view Event Log Statistics.

▶Remote Access Configuration

You can use this screen to select options for the Remote Access Configuration. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option.

Remote Access

This feature allows the user to disable the function of Remote Access. If "Disabled" is not select, then you can select a Remote Access type. The options are "Disabled" or "**Serial**".

Serial Port Number

Select the serial port you want to use for console redirection. You can set the value for this option to either "**COM1**" or "COM2".

Serial Port Mode

Select the baud rate you want the serial port to use for console redirection. Select "115200 8,n,1" to select 115200 as the baud rate (transmitted bits per second) of the serial port. Select "57600 8,n,1" to set 57600 as the baud rate (transmitted bits per second) of the serial port. Select "19200 8,n,1" to set 19200 as the baud rate (transmitted bits per second) of the serial port. The default setting is "**115200 8,n,1**".

Flow Control

Select the flow control for console redirection. You can set the value for this option to either "**None**" or "Hardware".

Terminal Type

This feature allows you to select the target terminal type. You can set the value for this option to either "**ANSI**" or "VT100".

Send Carriage Return

Select "Enabled" if the target terminal type has more than 80 columns or does not have the function of "Word Wrap". The options are "Enabled" and "**Disabled**".

Redirection After BIOS POST

Select "Disabled" to turn off the function of Console Redirection after POST. Select "Boot Loader" to keep the function of Redirection active during POST and during Boot Load. Select "Always" to keep the function of "Redirection" active all the time. If "Always" is selected, some operating systems might not function well The default setting is "**Boot Loader**".

▶Hardware Health Monitoring

H/W Health Function

Select "Enabled" to enable the function of Hardware Health Monitoring Device. The Options are "**Enabled**" and "Disabled".

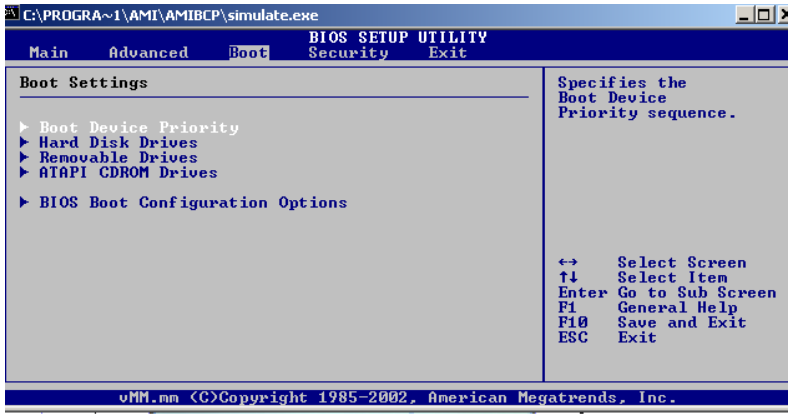
Overheat Temperature Trips

The feature allows the user to set the CPU temperature threshold. The options are "72ºC", "**78ºC**" and "85ºC.

4-4 Boot Settings

Boot Settings Configuration

Use this screen to select options for the Boot Settings Configuration. The settings are described on the following pages. The screen is shown below.



▶Boot Device Priority

This feature allows the user to specify the sequence of priority for the Boot Device.

The settings are "1st Floppy Drive", "CD ROM", "ATAPI CDROM", and "Disabled." The default settings are:

· 1st boot device –1st Floppy Drive

· 2nd boot device – CD ROM

· 3rd boot device – ATAPI CDROM

▶Hard Disk Drives

This feature allows the user to specify the Boot sequence from available Hard Drives.

1st Drive

Specify the boot sequence for 1st Hard Drive. The Options are "**PM-ST340016A**" and "Disabled".

▶Removable Drives

This feature allows the user to specify the Boot sequence from available Removable Drives.

1st Drive

Specify the boot sequence for 1st Removable Drive. The Options are "**1st Floppy Drive**" and "Disabled".

▶ATAPI Drives

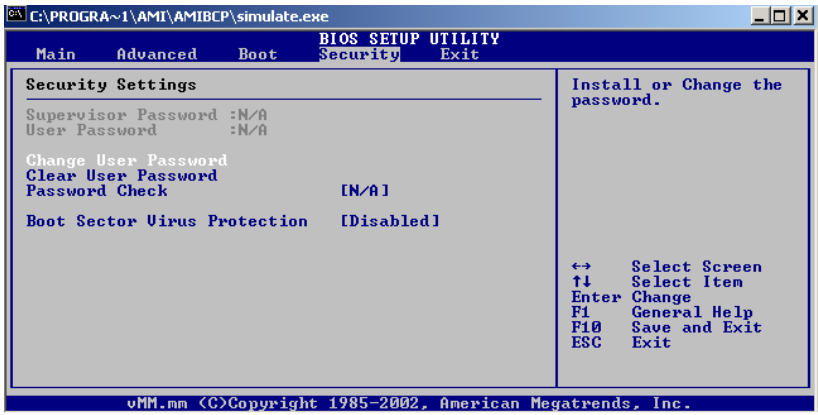
This feature allows the user to specify the boot sequence from available ATAPI CDROM Drives.

1st Drive

Specify the boot sequence for 1st Hard Drive. The Options are "**CD ROM**" and "Disabled".

4-5 Security Settings

AMI BIOS provides a Supervisor and a User password. If you use both passwords, the Supervisor password must be set first.



Change Supervisor Password

Select this option and press <Enter> to access the sub menu, and then, type in the password.

Change User Password

Select this option and press <Enter> to access the sub menu, and then, type in the password.

Clear User Password

Select this option and press <Enter> to access the sub menu. You can use the sub menu to clear the user password.

Boot Sector Virus Protection

This option is near the bottom of the Security Setup screen. Select "Disabled" to deactivate the Boot Sector Virus Protection. Select "Enabled" to enable boot sector protection. When "Enabled", AMI BOIS displays a warning when any program (or virus) issues a Disk Format command or attempts to write to the boot sector of the hard disk drive. The options are "Enabled" and "Disabled".

4-6 Exit Options

Select the Exit tab from the BIOS Setup Utility screen to enter the Exit BIOS Setup screen.

Save Changes and Exit

When you have completed the system configuration changes, select this option to leave BIOS Setup and reboot the computer, so the new system configuration parameters can take effect. Select Save Changes and Exit from the Exit menu and press <Enter>.

Discard Changes and Exit

Select this option to quit BIOS Setup without making any permanent changes to the system configuration and reboot the computer. Select Discard Changes and Exit from the Exit menu and press <Enter>.

Load Optimal Defaults

To set this feature, select Load Optimal Defaults from the Exit menu and press <Enter>. Then, Select "OK" to allow BIOS to automatically load Optimal Defaults to BIOS Settings. The Optimal settings are designed for maximum system performance, but may not work best for all computer applications.

Load Fail-Safe Defaults

To set this feature, select Load Fail-Safe Defaults from the Exit menu and press <Enter>. The Fail-Safe settings are designed for maximum system stability, but not maximum performance.

Appendix A
BIOS Error Beep Codes

During the POST (Power-On Self-Test) routines, which are performed each time the system is powered on, errors may occur.

Non-fatal errors are those which, in most cases, allow the system to continue the boot-up process. The error messages normally appear on the screen.

Fatal errors are those which will not allow the system to continue the boot-up procedure. If a fatal error occurs, you should consult with your system manufacturer for possible repairs.

These fatal errors are usually communicated through a series of audible beeps. The numbers on the fatal error list, on the following page, correspond to the number of beeps for the corresponding error. All errors listed, with the exception of Beep Code 8, are fatal errors.

POST codes may be read on the debug LEDs located beside the LAN port on the motherboard backplane. See the description of the Debug LEDs (LED1 and LED2) in Section 2-6.

A-1 AMIBIOS Error Beep Codes

Beep Code	Error Message	Description
1 beep	Refresh	Circuits have been reset. (Ready to power up.)
5 short, 1 long	Memory error	No memory detected in system
8 beeps	Display memory read/write error	Video adapter missing or with faulty memory

Notes

Appendix B
BIOS POST Checkpoint Codes

When AMIBIOS performs the Power On Self Test, it writes checkpoint codes to I/O port 0080h. If the computer cannot complete the boot process, diagnostic equipment can be attached to the computer to read I/O port 0080h.

B-1 Uncompressed Initialization Codes

The uncompressed initialization checkpoint codes are listed in order of execution:

Checkpoint	Code Description
D0h	The NMI is disabled. Power on delay is starting. Next, the initialization code checksum will be verified.
D1h	Initializing the DMA controller, performing the keyboard controller BAT test, starting memory refresh, and entering 4 GB flat mode next.
D3h	Starting memory sizing next.
D4h	Returning to real mode. Executing any OEM patches and setting the Stack next.
D5h	Passing control to the uncompressed code in shadow RAM at E000:0000h. The initialization code is copied to segment 0 and control will be transferred to segment 0.
D6h	Control is in segment 0. Next, checking if <Ctrl> <Home> was pressed and verifying the system BIOS checksum. If either <Ctrl> <Home> was pressed or the system BIOS checksum is bad, next will go to checkpoint code E0h. Otherwise, going to checkpoint code D7h.

B-2 Bootblock Recovery Codes

The bootblock recovery checkpoint codes are listed in order of execution:

Checkpoint	Code Description
E0h	The onboard floppy controller if available is initialized. Next, beginning the base 512 KB memory test.
E1h	Initializing the interrupt vector table next.
E2h	Initializing the DMA and Interrupt controllers next.
E6h	Enabling the floppy drive controller and Timer IRQs. Enabling internal cache memory.
Edh	Initializing the floppy drive.
Eeh	Looking for a floppy diskette in drive A:. Reading the first sector of the diskette.
Efh	A read error occurred while reading the floppy drive in drive A:.
F0h	Next, searching for the AMIBOOT.ROM file in the root directory.
F1h	The AMIBOOT.ROM file is not in the root directory.
F2h	Next, reading and analyzing the floppy diskette FAT to find the clusters occupied by the AMIBOOT.ROM file.
F3h	Next, reading the AMIBOOT.ROM file, cluster by cluster.
F4h	The AMIBOOT.ROM file is not the correct size.
F5h	Next, disabling internal cache memory.
FBh	Next, detecting the type of flash ROM.
FCh	Next, erasing the flash ROM.
FDh	Next, programming the flash ROM.
FFh	Flash ROM programming was successful. Next, restarting the system BIOS.

B-3 Uncompressed Initialization Codes

The following runtime checkpoint codes are listed in order of execution. These codes are uncompressed in F0000h shadow RAM.

Checkpoint	Code Description
03h	The NMI is disabled. Next, checking for a soft reset or a power on condition.
05h	The BIOS stack has been built. Next, disabling cache memory.
06h	Uncompressing the POST code next.
07h	Next, initializing the CPU and the CPU data area.
08h	The CMOS checksum calculation is done next.
0Ah	The CMOS checksum calculation is done. Initializing the CMOS status register for date and time next.
0Bh	The CMOS status register is initialized. Next, performing any required

	initialization before the keyboard BAT command is issued.
0Ch	The keyboard controller input buffer is free. Next, issuing the BAT command to the keyboard controller.
0Eh	The keyboard controller BAT command result has been verified. Next, performing any necessary initialization after the keyboard controller BAT command test.
0Fh	The initialization after the keyboard controller BAT command test is done. The keyboard command byte is written next.
10h	The keyboard controller command byte is written. Next, issuing the Pin 23 and 24 blocking and unblocking command.
11h	Next, checking if <End or <Ins> keys were pressed during power on. Initializing CMOS RAM if the *Initialize CMOS RAM in every boot* AMIBIOS POST option was set in AMIBCP or the <End> key was pressed.
12h	Next, disabling DMA controllers 1 and 2 and interrupt controllers 1 and 2.
13h	The video display has been disabled. Port B has been initialized. Next, initializing the chipset.
14h	The 8254 timer test will begin next.
19h	The 8254 timer test is over. Starting the memory refresh test next.
1Ah	The memory refresh line is toggling. Checking the 15 second on/off time next.
2Bh	Passing control to the video ROM to perform any required configuration before the video ROM test.
2Ch	All necessary processing before passing control to the video ROM is done. Looking for the video ROM next and passing control to it.
2Dh	The video ROM has returned control to BIOS POST. Performing any required processing after the video ROM had control.
23h	Reading the 8042 input port and disabling the MEGAKEY Green PC feature next. Making the BIOS code segment writable and performing any necessary configuration before initializing the interrupt vectors.
24h	The configuration required before interrupt vector initialization has completed. Interrupt vector initialization is about to begin.

Checkpoint	Code Description
25h	Interrupt vector initialization is done. Clearing the password if the POST DIAG switch is on.
27h	Any initialization before setting video mode will be done next.
28h	Initialization before setting the video mode is complete. Configuring the monochrome mode and color mode settings next.
2Ah	Bus initialization system, static, output devices will be done next, if present. See the last page for additional information.
2Eh	Completed post-video ROM test processing. If the EGA/VGA controller is not found, performing the display memory read/write test next.
2Fh	The EGA/VGA controller was not found. The display memory read/write test is about to begin.
30h	The display memory read/write test passed. Look for retrace checking next.
31h	The display memory read/write test or retrace checking failed. Performing the alternate display memory read/write test next.
32h	The alternate display memory read/write test passed. Looking for alternate display retrace checking next.
34h	Video display checking is over. Setting the display mode next.
37h	The display mode is set. Displaying the power on message next.
38h	Initializing the bus input, IPL, general devices next, if present. See the last page of this chapter for additional information.
39h	Displaying bus initialization error messages. See the last page of this chapter for additional information.
3Ah	The new cursor position has been read and saved. Displaying the *Hit <DEL>* message next.
3Bh	The *Hit <DEL>* message is displayed. The protected mode memory test is about to start.
40h	Preparing the descriptor tables next.
42h	The descriptor tables are prepared. Entering protected mode for the memory test next.
43h	Entered protected mode. Enabling interrupts for diagnostics mode next.
44h	Interrupts enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0 next.
45h	Data initialized. Checking for memory wraparound at 0:0 and finding the total system memory size next.
46h	The memory wraparound test is done. Memory size calculation has been done. Writing patterns to test memory next.
47h	The memory pattern has been written to extended memory. Writing patterns to the base 640 KB memory next.

Checkpoint	Code Description
48h	Patterns written in base memory. Determining the amount of memory below 1 MB next.
49h	The amount of memory below 1 MB has been found and verified. Determining the amount of memory above 1 MB memory next.
4Bh	The amount of memory above 1 MB has been found and verified. Checking for a soft reset and clearing the memory below 1 MB for the soft reset next. If this is a power on situation, going to checkpoint 4Eh next.
4Ch	The memory below 1 MB has been cleared via a soft reset. Clearing the memory above 1 MB next.
4Dh	The memory above 1 MB has been cleared via a soft reset. Saving the memory size next. Going to checkpoint 52h next.
4Eh	The memory test started, but not as the result of a soft reset. Displaying the first 64 KB memory size next.
4Fh	The memory size display has started. The display is updated during the memory test. Performing the sequential and random memory test next.
50h	The memory below 1 MB has been tested and initialized. Adjusting the displayed memory size for relocation and shadowing next.
51h	The memory size display was adjusted for relocation and shadowing. Testing the memory above 1 MB next.
52h	The memory above 1 MB has been tested and initialized. Saving the memory size information next.
53h	The memory size information and the CPU registers are saved. Entering real mode next.
54h	Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next.
57h	The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next.
58h	The memory size was adjusted for relocation and shadowing. Clearing the *Hit* <*DEL*> message next.
59h	The *Hit* <*DEL*> message is cleared. The <*WAIT...*> message is displayed. Starting the DMA and interrupt controller test next.

Checkpoint	Code Description
60h	The DMA page register test passed. Performing the DMA Controller 1 base register test next.
62h	The DMA controller 1 base register test passed. Performing the DMA controller 2 base register test next.
65h	The DMA controller 2 base register test passed. Programming DMA controllers 1 and 2 next.
66h	Completed programming DMA controllers 1 and 2. Initializing the 8259 interrupt controller next.
67h	Completed 8259 interrupt controller initialization.
7Fh	Extended NMI source enabling is in progress.
80h	The keyboard test has started. Clearing the output buffer and checking for stuck keys. Issuing the keyboard reset command next.
81h	A keyboard reset error or stuck key was found. Issuing the keyboard controller interface test command next.
82h	The keyboard controller interface test completed. Writing the command byte and initializing the circular buffer next.
83h	The command byte was written and global data initialization has completed. Checking for a locked key next.
84h	Locked key checking is over. Checking for a memory size mismatch with CMOS RAM data next.
85h	The memory size check is done. Displaying a soft error and checking for a password or bypassing WINBIOS Setup next.
86h	The password was checked. Performing any required programming before WINBIOS Setup next.
87h	The programming before WINBIOS Setup has completed. Uncompressing the WINBIOS Setup code and executing the AMIBIOS Setup or WINBIOS Setup utility next.
88h	Returned from WINBIOS Setup and cleared the screen. Performing any necessary programming after WINBIOS Setup next.
89h	The programming after WINBIOS Setup has completed. Displaying the power on screen message next.
8Bh	The first screen message has been displayed. The <*WAIT...*> message is displayed. Performing the PS/2 mouse check and extended BIOS data area allocation check next.
8Ch	Programming the WINBIOS Setup options next.
8Dh	The WINBIOS Setup options are programmed. Resetting the hard disk controller next.
8Fh	The hard disk controller has been reset. Configuring the floppy drive controller next.
91h	The floppy drive controller has been configured. Configuring the hard disk drive controller next.

Checkpoint	Code Description
95h	Initializing the bus option ROMs from C800 next. See the last page of this chapter for additional information.
96h	Initializing before passing control to the adaptor ROM at C800.
97h	Initialization before the C800 adaptor ROM gains control has completed. The adaptor ROM check is next.
98h	The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control.
99h	Any initialization required after the option ROM test has completed. Configuring the timer data area and printer base address next.
9Ah	Set the timer and printer base addresses. Setting the RS-232 base address next.
9Bh	Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test next.
9Ch	Required initialization before the Coprocessor test is over. Initializing the Coprocessor next.
9Dh	Coprocessor initialized. Performing any required initialization after the Coprocessor test next.
9Eh	Initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next.
A2h	Displaying any soft errors next.
A3h	The soft error display has completed. Setting the keyboard typematic rate next.
A4h	The keyboard typematic rate is set. Programming the memory wait states next.
A5h	Memory wait state programming is over. Clearing the screen and enabling parity and the NMI next.
A7h	NMI and parity enabled. Performing any initialization required before passing control to the adaptor ROM at E000 next.
A8h	Initialization before passing control to the adaptor ROM at E000h completed. Passing control to the adaptor ROM at E000h next.
A9h	Returned from adaptor ROM at E000h control. Performing any initialization required after the E000 option ROM had control next.
Aah	Initialization after E000 option ROM control has completed. Displaying the system configuration next.
Abh	Uncompressing the DMI data and executing DMI POST initialization next.
B0h	The system configuration is displayed.
B1h	Copying any code to specific areas.
00h	Code copying to specific areas is done. Passing control to INT 19h boot loader next.

Notes