



MEMORY RAS CONFIGURATION

USER'S GUIDE

Revision 1.0

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Chapter 1

Introduction

About This User Guide

This user's guide is written for system integrators, IT technicians, and knowledgeable end users. It provides information on memory RAS support and configuration on a Supermicro motherboard or system.

Introduction to Reliability, Availability and Serviceability

Reliability, Availability, and Serviceability (RAS) is a computer-engineering architecture that promotes reliability engineering, high availability, and serviceability design. For product reliability, computer components or systems are designed to maintain consistent performance based on the specifications without deviations or errors. For system availability, a component or server will always function as it should, and it will also be constantly available for use with minimal downtime. For computer serviceability, a component or a system can be maintained or repaired with ease. With full implementation of RAS into our product design and system integration, Supermicro's computer systems are engineered to provide you with the highest standards in quality, performance, availability, and usability at all times.

Introduction to Memory RAS Configuration

As a world's server manufacturer leader, Supermicro has integrated memory RAS features into our products to enhance data integrity and system performance and to prevent data alternation or data loss caused by electronic transactions for many years. Additionally, we've also built in layers of data-checking, error-detection, and error-correction mechanisms for memory error recovery to maximize storage and network security. The memory RAS capabilities that have been implemented into our products include memory mirroring, enhanced Error Checking and Correction (ECC), memory scrubbing, and memory sparing. In addition to these highly efficient memory protection mechanisms that are embedded in the integrated memory controllers of Supermicro computers, we've utilized the latest technology available in the industry to further enhance data integrity and system security for our systems. These new advanced RAS features include:

- SDDC: Single Device Data Correction
- SDDC+1: SDDC_Plus_One
- DDDC: Double Device Data Correction
- ADDDC: Adaptive Double Device Data Correction

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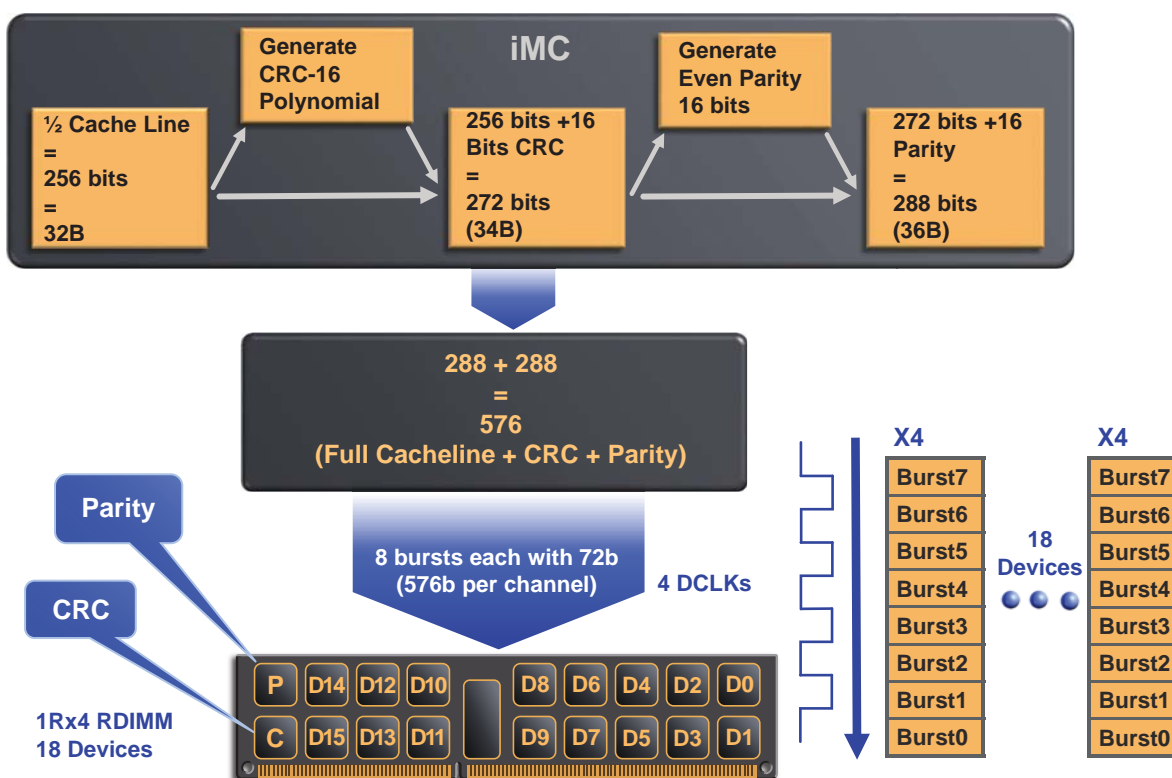
Intel ECC Mode Common Technology

SDDC

Single Device Data Correction (SDDC) checks and corrects single-bit or multiple-bit (4-bit max.) memory faults that affect an entire single x4 DRAM device.

SDDC Algorithm Overview (1 of 3)

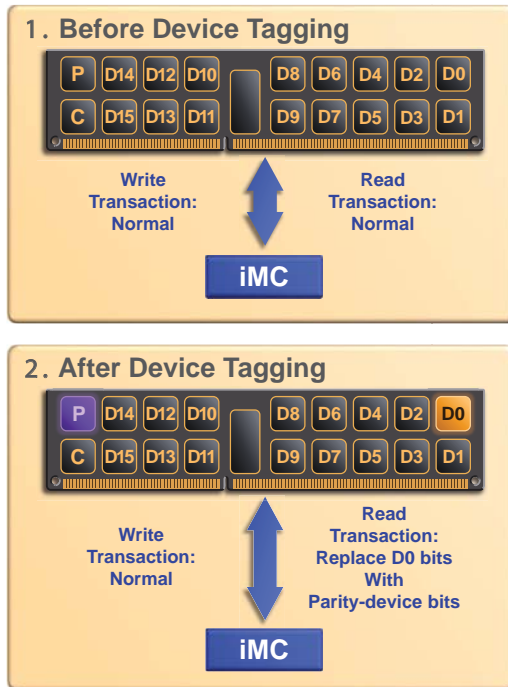
Memory Write with CRC and Parity bits encoding



SDDC + 1

SDDC+1, which is the enhanced feature to SDDC, will spare the faulty DRAM device out after an SDDC event has occurred. After the event, the SDDC+1 ECC mode is activated to protect against any additional memory failure caused by a 'single-bit' error in the same memory rank.

SDDC+1 Algorithm with Device Tagging



1. Normal Memory Write/Read
2. Example: Device D0 hard failure.
 1. Corrected Error Count would reach threshold quickly.
 2. BIOS/SMM detects the failed DRAM Device D0. Triggers Device Tagging.

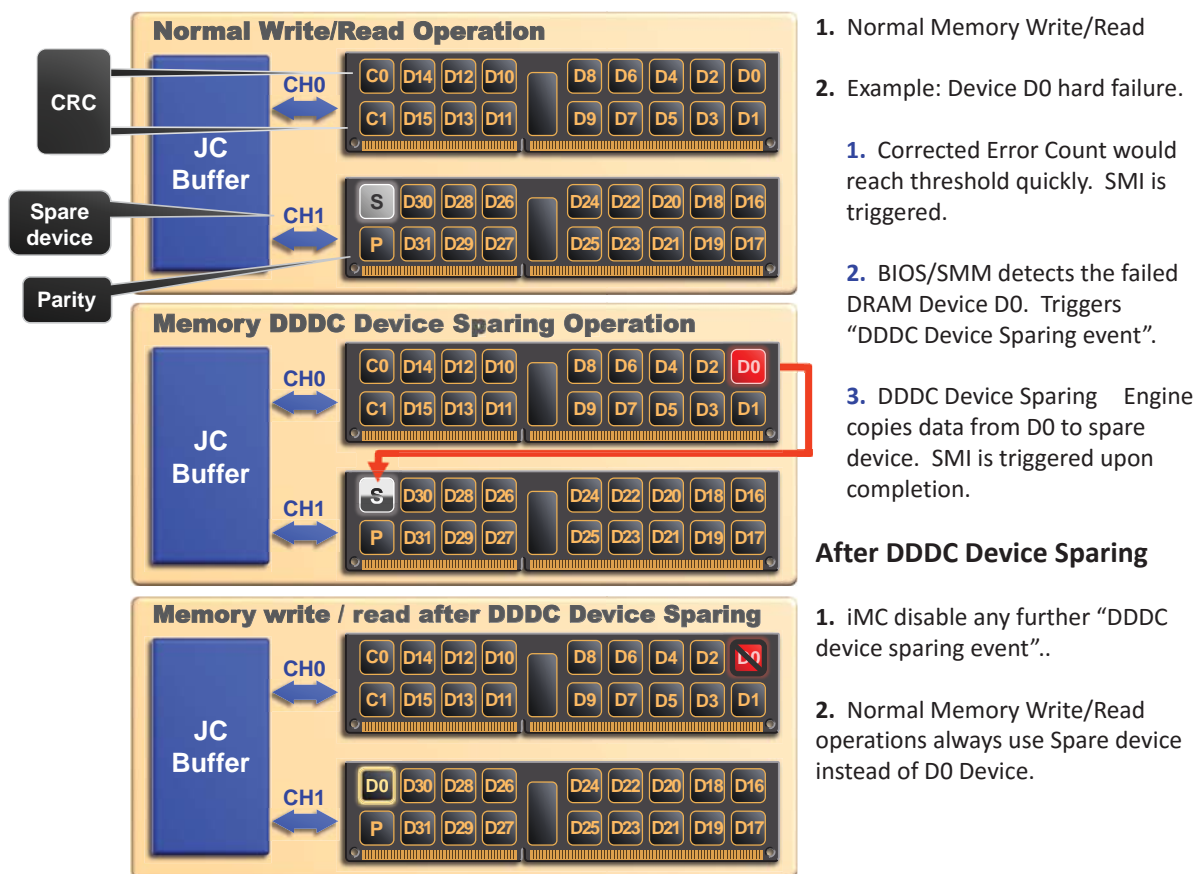
After Device Tagging

1. Memory Writer operation: Unchanged (Normal).
2. Memory read operation:
 1. D0 device data is replaced with that of Parity Device.
 2. iMC does normal error Checking.
 3. Intel Xeon Scalable Processor Family: Upon detecting error, logs error and signal MCE.

DDDC

Double Device Data Correction (DDDC) provides error checking and correction to protect against memory failures occurred to two, sequential, and x4 DRAM devices due to hard-errors on DIMM modules. DDDC is supported only with x4 DRAMs and with two channels in the lockstep mode. (This feature is not supported for x8 DRAM device-based DIMM.)

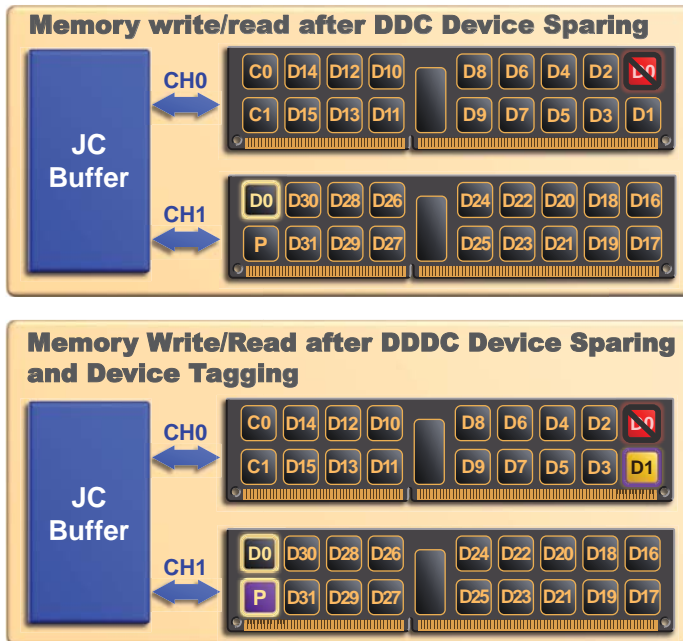
Memory DDDC+1 Algorithm Overview (2 of 3)



DDDC+1

Double Device Data Correction (DDDC) Plus One allows the error correction code to correct an error caused by the failure of two DRAM devices or by a single-bit error that is beyond a device failure in the lockstep mode.

Memory DDDC+1 Algorithm Overview (3 of 3)



1. Normal Memory Write/Read with Spare Device as D0.

2. Example: Device D1 hard failure (second device).

1. Corrected Error Count would reach threshold quickly.

2. BIOS/SMM detects the failed DRAM Device D1. Triggers Device Tagging.

After DDDC Device Sparing

1. Memory Write operation: Unchanged. Still using spare device.

2. Memory read operation:

1. D1 device data is replaced with that of Parity Device.

2. iMC does normal error checking.

3. Upon detecting error, logs error and corrects SBE. In case of MBE, logs error and signal MCE.

ADDDC

Adaptive Double Device Data Correction (ADDDC), which is an enhanced feature to DDDC, will not issue a performance penalty before a device fails. Please note that virtual lockstep mode will only start to work for ADDDC after a faulty DRAM module is spared out at Bank or Rank granularity.

ADDDC+1 (Adaptive Double Device Data Correction Plus One)

Adaptive Double Device Data Correction Plus One (ADDDC+1), which is an improved feature of ADDDC, will allow the error correction code to correct an error caused by the failure of two DRAM devices or by a single-bit error that is beyond a device failure in the lockstep mode. ADDDC+1 will not issue a performance penalty before a device fails. Please note that virtual lockstep mode will only start to work for ADDDC after a faulty DRAM module is spared out at Bank granularity or Rank granularity.

ADDDC (Adaptive Double Device Correction) Bank

If ADDDC Bank is implemented, a memory failure will only occur to a DRAM bank and will not occur to the whole device because a bank granularity of a DRAM region will enter into virtual lockstep (VLS) along with a buddy bank, allowing the content of the bank of a failing DRAM device to be copied over to the bank of the spare buddy device as soon as an error occurs to a good DIMM.

Adaptive DDDC (MR), Bank Virtual lockstep

First Strike Rank A, Device 0, Bank 0

| B a n k I D | Rank A | | | | | | | | | | | | | | | | | |
|----------------------------|--------------|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | X4 Device ID | | | | | | | | | | | | | | | | | |
| | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | |
| n | | | | | | | | | | | | | | | | | | |

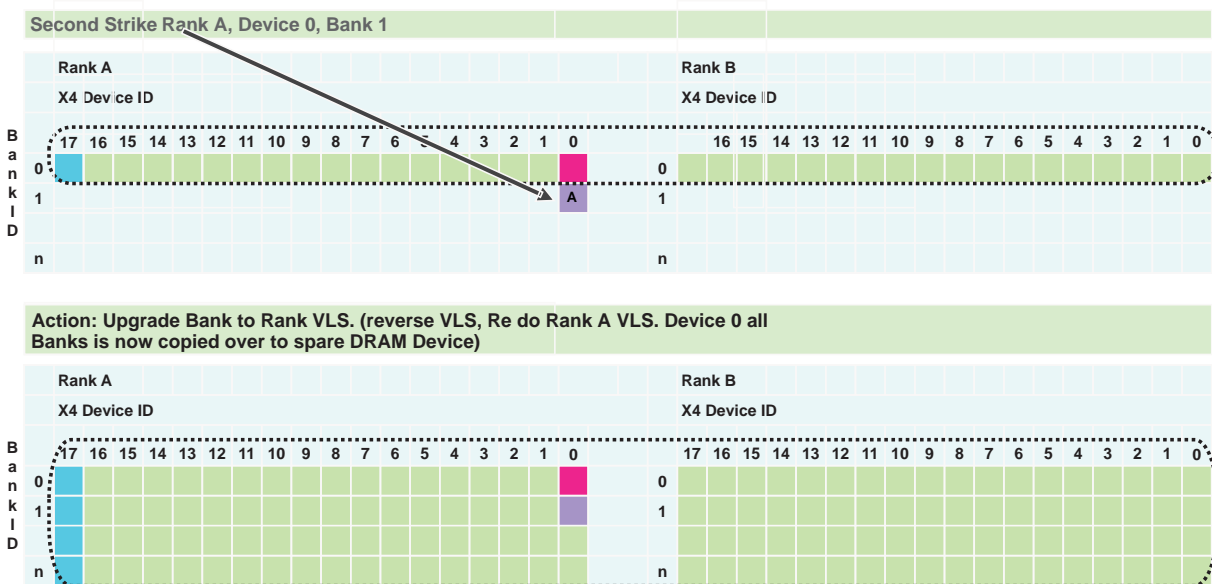
Action: VLS the failed Bank, map out Device 0, Bank 0 by copying Content to bank 0 in spare DRAM Device.

| Bank ID | Rank A | | | | | | | | | | | | | | | | | | Rank B | | | | | | | | | | | | | | | | | |
|---------|--------------|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--------------|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | X4 Device ID | | | | | | | | | | | | | | | | | | X4 Device ID | | | | | | | | | | | | | | | | | |
| | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| n | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

ADDDC (Adaptive Double Device Correction) Rank

If ADDDC Rank is implemented, device sparing at a rank granularity will be enabled to allow the content of the whole DRAM device to be copied to a spare device when a second saved DRAM device installed in another bank of the same memory channel fails.

Adaptive DDDC (MR), Second Strike Rank A

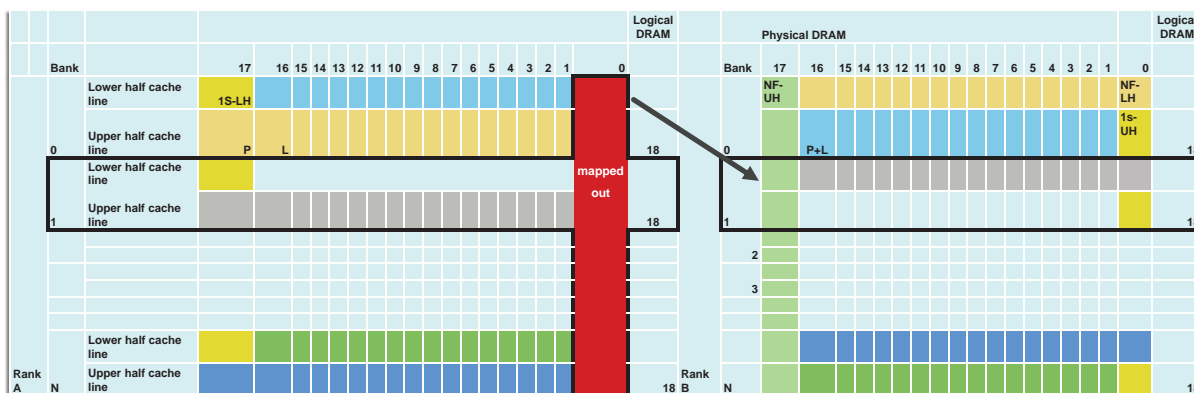


SDDC + 1

- *SDDC + 1 will occur* if 'ADDDC spare' is enabled in the BIOS menu. This will only happen when another 'single device failure' occurs after an "ADDDC Rank" event, and the current ECC mode can correct an additional single bit error after SDDC spare is completed;
- *SDDC + 1 will occur* if 'ADDDC spare' is disabled, 'SDDC plus one' is enabled in the BIOS menu, and VLS is disabled. This mode is enabled after 'a single DRAM device failure' has occurred and the process of 'device spare' is completed. It can correct an additional single bit error in the ECC mode.
- *SDDC + 1 will occur* when a correctable memory error within one DRAM device bank exceeds the threshold, and ADDDC Bank Virtual Lock Step is active. Subsequently, a correctable memory error in any other bank will trigger "ADDDC Rank Virtual Lock Step", and it will trigger SDDC+1 in any other DRAM device as well.

Physical/Logical DRAM Map, Rank VLS

Physical/logical DRAM Map, Rank VLS



Post Rank VLS: DRAM 0 is mapped out, Rank B device 17 holds Data
Parity+Locator is combined into Device 16.

Memory RAS DIMM Limitation

| Memory RAS DIMM Limitation | | |
|----------------------------|---------------|-------------------|
| DRAM Type | x4 DRAM DIMMS | x8 DRAM DIMM |
| SDDC(+1) | Support | Support (Note *1) |
| ADDDC(+1) | Support | Not Support |

Note 1: x8 Single Device Data Correction (SDDC) and SDDC+1 are supported only via 'static virtual lockstep'. Please be sure to enable 'Static Virtual Lockstep Mode' in the BIOS setup utility. Please be sure to install at least one x8DIMM module with two logical RANKs or two x8 DIMM modules with a single RANK each in a DDR channel.

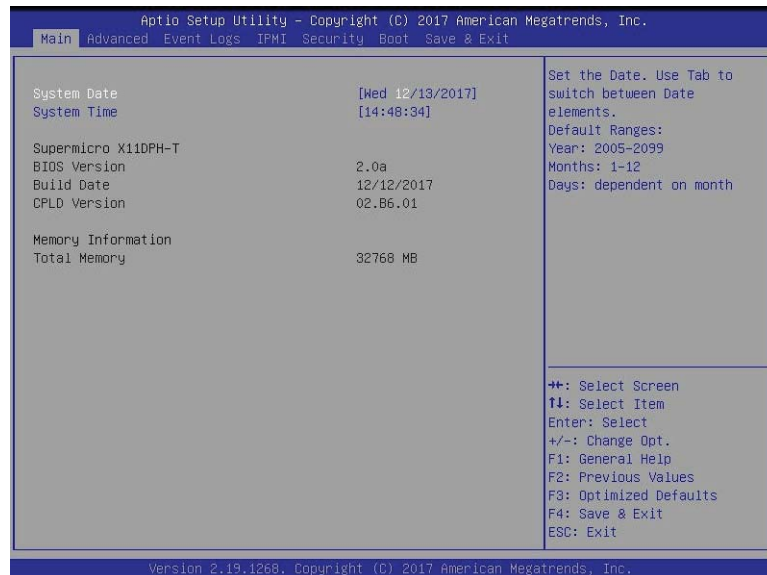
Note 2: SDDC (+1) and ADDDC (+1) are not compatible with Mirroring and Rank Sparring. When Mirror or Rank Sparring is enabled, neither ADDDC nor SDDC will not be supported.

Chapter 3

Configuring Memory RAS Features in the BIOS Setup Utility

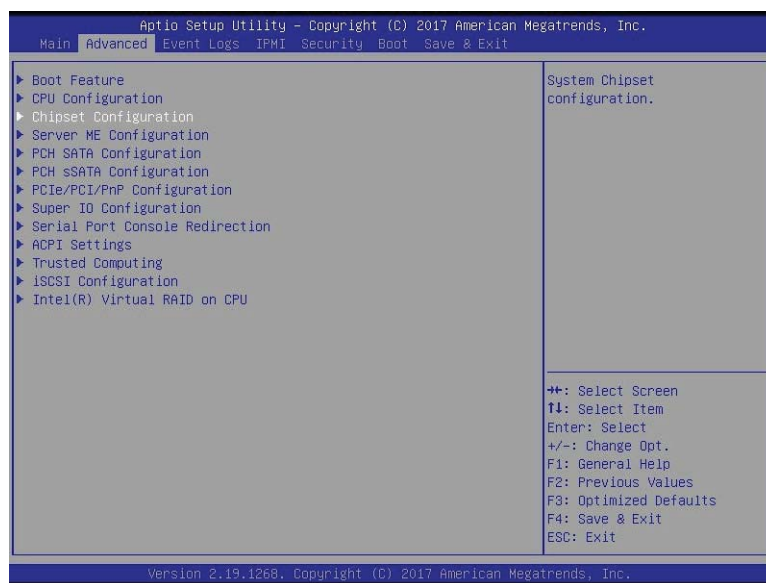
To configure the SDDC+1/ADDDC RAS settings in the BIOS, follow the instructions below:

1. Power on your computer and hit the <Delete> key continuously to enter the BIOS setup utility upon bootup as the screen shown below.

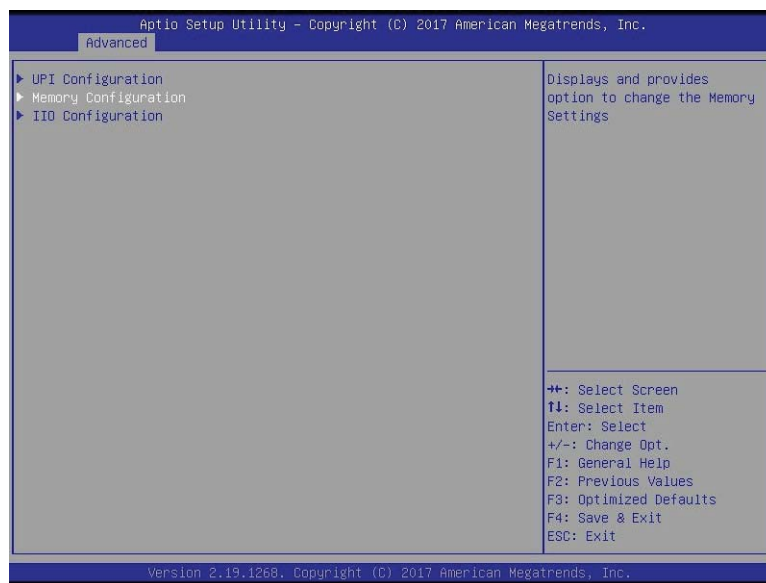


2. Using the arrow keys, select the <Advanced> menu on the top of the screen and hit <Enter> to enter the Advanced submenu.

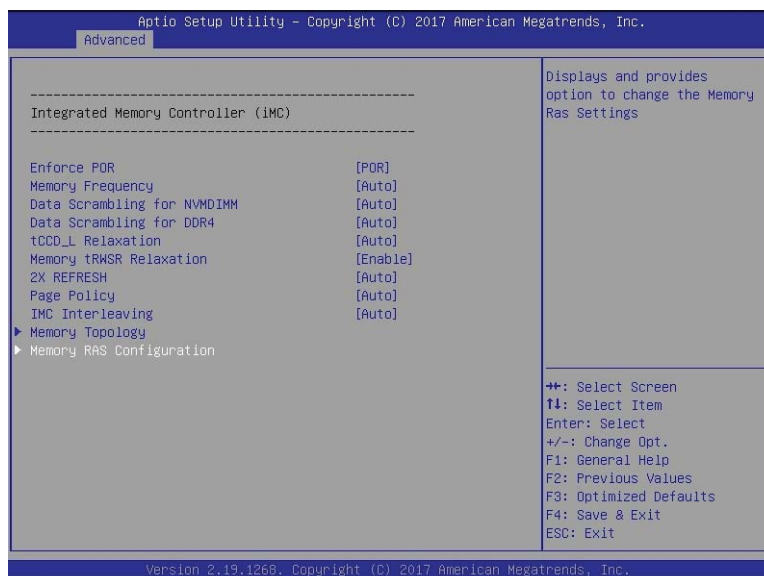
3. Using the down arrow key, scroll down to select the *Chipset Configuration* submenu and hit <Enter> as shown below.



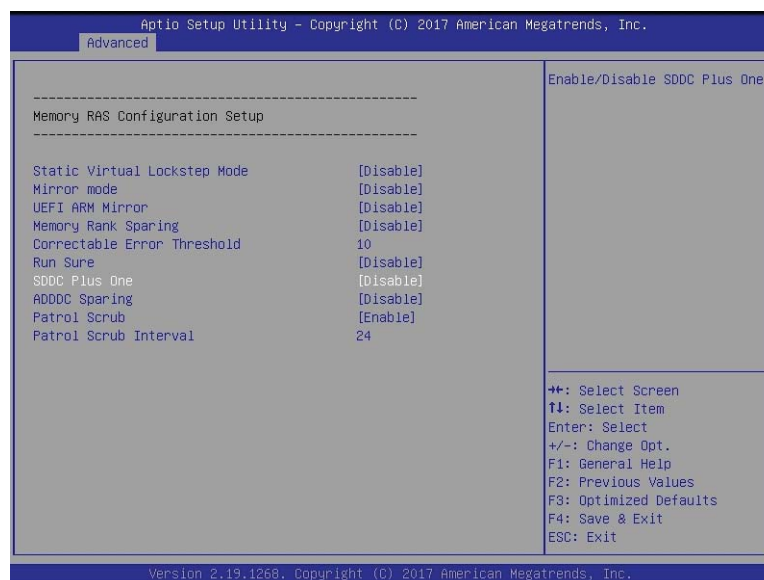
4. Select *North Bridge* and hit <Enter>. The following screen will display.



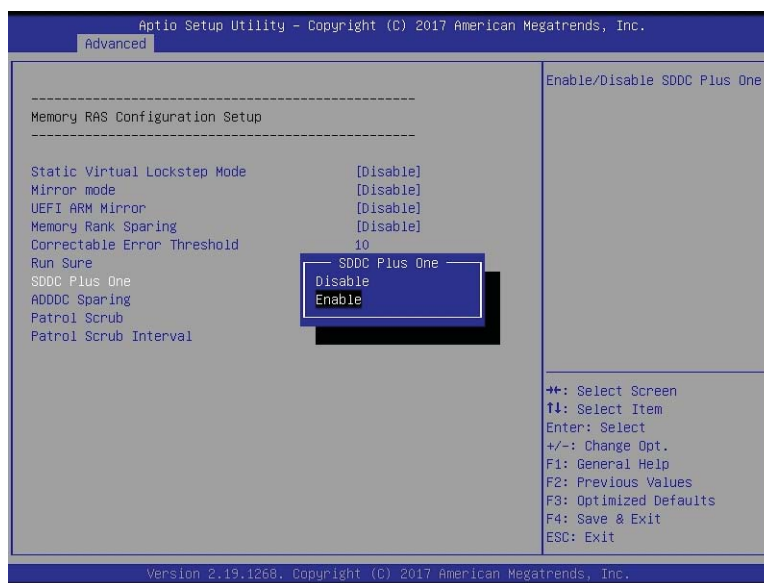
5. Use the arrow key to select *Memory Configuration* and hit <Enter>. The following screen will display.



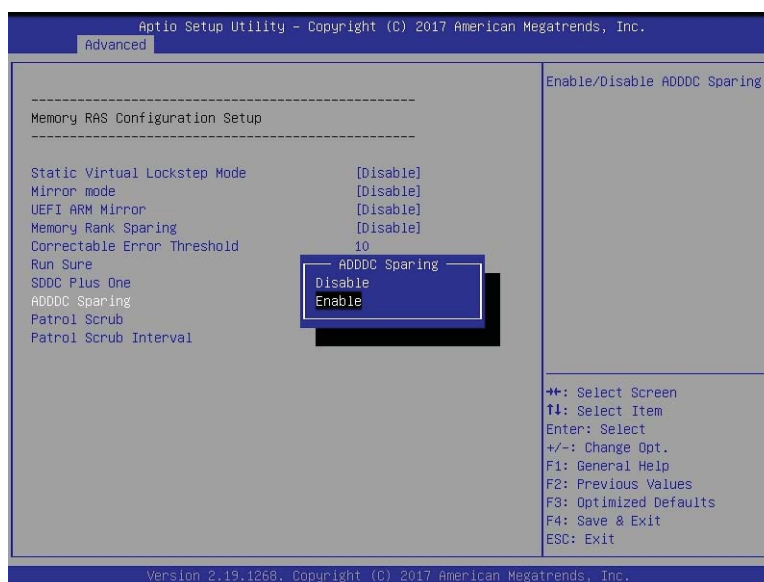
6. Using the down arrow key, scroll down to select *Memory RAS Configuration* from the screen above and hit <Enter>. The following screen will display:



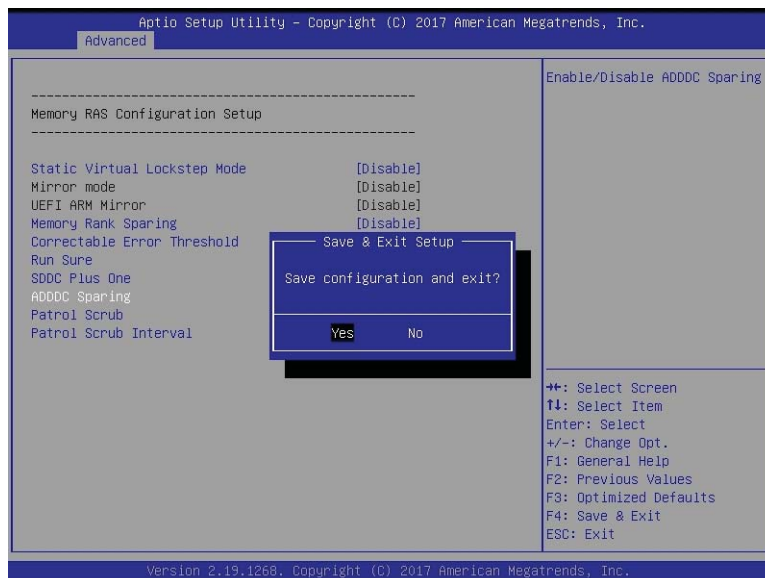
7. Select *SDDC Plus One* and hit <Enter>. The options for SDDC Plus One will display as shown below. Using the arrow keys select *Enable* and hit <Enter>.



8. Scroll down to *ADDDC Sparing* and hit <Enter>. Select *Enable* and hit <Enter> as shown below.



9. Once you've set both items: *SDDC Plus One* and *ADDDC Sparing* to Enable, press the <F4> key on the top of your keyboard to save your configuration settings and exit the BIOS setup utility as shown below.



10. Reboot your system for the new configuration settings to take effect.