

IPMI Firmware / BIOS Release Notes Form

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| Product Name | X10DRW-i(T) |
| Release Version | 3.0a |
| Release Date | 2/8/2018 |
| Previous Version | 2.0b |
| Update Category | Critical |
| Dependencies | None |
| Important Notes | None |
| Enhancements | <ol style="list-style-type: none">1. Updated SATA RAID OPRM/EFI driver to RSTe PreOS v4.7.0.1014.2. Updated Intel Server Platform Services 3.1.3.50 for Grantley Refresh Platforms.3. Updated CPU microcode SRV_B_204 for Haswell-EP C0,1/M0,1/R2 & Broadwell-EP B0/M0/R0.4. Removed support for using Ctrl+home to trigger recovery.5. Changed BIOS revision to 3.0a.6. Changed Memory correctable threshold to 100 and enabled Cloaking for Broadwell CPU E5-26xx SKU.7. Updated Broadwell-EP RC 4.3.0 PLR10 release.8. Updated BIOS ACM 3.1.1 PW and SINIT ACM 3.1.1 PW.9. Added BBS reset function to SmcOobLoadBiosDefault().10. Changed tCCD_L Relaxation default to 1 and changed string from Enabled to Auto. |

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| | <p>11. Appended VPD - VB tag in VPD-W Tag(0x91) area.</p> <p>12. Added SumBbsSupportFlag into DAT file.</p> <p>13. Added support for JEDEC NVDIMM.</p> <p>14. Added support for LSI 3008/3016 HBA sensor.</p> <p>15. Updated new MRC error log definition.</p> <p>16. Added Intel SPI vulnerability patch for Grantley.</p> <p>17. Updated Broadwell-EP B0/M0/R0 CPU uCode MEF406F1_0B000022.</p> <p>18. Added "SMBIOS Preservation" Enabled/Disabled item for flash recovery.</p> <p>19. Enhanced SMC Recovery Flash Boot Block feature.</p> |
| New features | <p>1. Implemented SMC Recovery Flash Boot Block feature.</p> |
| Fixes | <p>1. Fixed missing Manufacturer string in SMBIOS type 17 when Ramaxel DIMM is plugged in.</p> <p>2. Fixed problem of NVDIMM setup items appearing when optimized defaults load even without NVDIMM being installed.</p> <p>3. Fixed problem of SMBIOS Type4 CPU2 current speed not showing as zero when CPU2 is not installed.</p> <p>4. Fixed problem of system resetting or hanging after Watch Dog function is enabled during BIOS update.</p> <p>5. Fixed inability to get correct Memory CECC DIMM location via SD5.</p> |

Release Notes from Previous Release(s) – these will be appended at the bottom of the current release notes in italic and in smaller print