

IPMI Firmware / BIOS Release Notes Form

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Product Name	X10DRC(-I/LN4+/T4+)
Release Version	3.0a
Release Date	2/9/2018
Previous Version	2.0b
Update Category	Critical
Dependencies	None
Important Notes	None
Enhancements	<ol style="list-style-type: none">1. Implemented enhancement to address 'Spectre' variant 2 (CVE 2017-5715) security patch issue.2. Changed BIOS revision to 3.0a.3. Updated Intel Server Platform Services 3.1.3.50 for Grantley Refresh Platforms.4. Updated SATA RAID OPRM/EFI driver to RSTe PreOS v4.7.0.1014 (RSTe SATA 4.7.0.1069 and NVMe 4.7.0.2063).5. Removed support for using Ctrl+home to trigger recovery.6. Added support for UEFI mode PXE boot via F12 hot key Net boot.7. Fixed inability of SUM utility to get "Setup Prompt Timeout" setup item.8. Updated Broadwell-EP RC 4.3.0 PLR11 release.9. Displayed setup item "ACS Control" to Enable/Disable PCIe Access Control Services Extended Capability.

	<p>10. Updated BIOS ACM 3.1.1 PW and SINIT ACM 3.1.1 PW.</p> <p>11. Added tCCD_L Relaxation item under Memory Configuration menu.</p> <p>12. Added SumBbsSupportFlag into DAT file.</p> <p>13. Added Intel SPI vulnerability patch for Grantley.</p> <p>14. Added "SMBIOS Preservation" Enabled/Disabled item for flash recovery.</p> <p>15. Enhanced SMC Recovery Flash Boot Block feature.</p>
New features	<p>1. Added support for JEDEC NVDIMM.</p> <p>2. Implemented SMC Recovery Flash Boot Block feature.</p>
Fixes	<p>1. Updated FlashDriver module to Label 5 in order to fix inability of system to enter recovery mode when MAIN block is updated 45% and then system powers off.</p> <p>2. Added Ramaxel JEDEC ID to support Ramaxel memory.</p> <p>3. Fixed problem of NVDIMM setup items appearing when optimized defaults load even without NVDIMM being installed.</p> <p>4. Corrected POST diagnostic signOn string.</p> <p>5. Fixed problem of SMBIOS Type4 CPU2 current speed not showing as zero when CPU2 is not installed.</p> <p>6. Fixed problem of system resetting or hanging after Watch Dog function is enabled during BIOS update.</p> <p>7. Fixed problem of MWAIT being disabled on BSP only.</p> <p>8. Fixed inability to get correct Memory CECC DIMM location via SD5.</p>