IPMI Firmware / BIOS Release Notes Form

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Product Name	X10SRH-C(LN4)F
Release Version	3.1c
Release Date	5/2/2019
Previous Version	3.1
Update Category	Recommended
Dependencies	None
Important Notes	None
Enhancements	1. Changed BIOS revision to 3.1c.
	2. Updated Intel Server Platform Services 3.1.3.72 for Grantley
	Refresh Platforms for INTEL-SA-00213 Security Advisory to address
	CVE-2019-0089, CVE-2019-0090, CVE-2019-0086, CVE-2019-0091, CVE-
	2019-0092, CVE-2019-0093, CVE-2019-0094, CVE-2019-0096, CVE-
	2019-0097, CVE-2019-0098, and CVE-2019-0099 security issues.
	3. Updated Haswell-EP/Broadwell-EP CPU microcode from
	SRV_P_273 for INTEL-SA-00233 Security Advisory to address CVE-
	2018-12126, CVE-2018-12127, and CVE-2018-12130 security issues.
	4. Forced a global reset if SPI descriptor is not write-protected after
	BIOS flash.
	5. Implemented anti-rollback for FDT Read-Only.
	6. Implemented multi-line IPMI page text and string.
	7. Updated EIP393007 & EIP411789 for TPM vulnerability when

	resuming S3.
	8. Updated SATA/sSATA RAID OPROM/EFI driver to VROC PreOS
	v6.1.0.1017.
	9. Updated VBIOS and VGA EFI Driver to 1.09 to fix ASpeed CVE-2019-
	6260 security issue.
	10. Updated valid range of IPMI setup item VLAN ID to 1-4094.
	11. Added support for RFC4122 UUID format feature to set RFC4122
	encoding from build time produced by IPMICFG 1.29 tool or newer.
	12. Added support for setting IPv6 Static Router1 prefix length and
	value in BIOS setup menu feature.
New features	N/A
	1. Fixed problem of BIOS always retrying boot when Re-Try Boot is
Fixes	Disabled.
	2. Fixed malfunction of METW if many error events are triggered
	within a very short time.
	3. Displayed the driver health support pages to support LSI
	(Broadcom 9440-8i) driver health status.
	4. Fixed malfunction of Windows Consistent Device Naming (CDN).

Release Notes from Previous Release(s)

3.1 (6/6/2018)

1. Updated CPU microcode to address 'Spectre' derivatives (CVE-2018-3639 & CVE-2018-3640) security issue.

2. Changed BIOS version to 3.1.

3. Added support for IPMI IPV6.

4. Removed unsupported memory frequency options from setup menu.

5. Updated Broadwell-EP RC 4.4.0 release.

6. Fixed problem of Afu /O command clearing SMC SMBIOS region (\$SMC).

7. Fixed problem of SUM OOB GetSataInfo always showing "Configuration Type" as "AHCI" when setting "Configure SATA as" to "RAID" or "IDE".

8. Fixed failure of SMBIOS to change to default even if preserve SMBIOS setup item is set to disabled during recovery.

9. Fixed problem of the system debug card hanging at 79h after setting JBR1 to pins 2-3 (BIOS RECOVERY).

10. Set Descriptor Region of BIOS Region Write Access to "No".

3.0a (02/08/2018)

1. Updated Haswell-EP C0,1/M0,1/R2 CPU microcode M6F306F2_0000003C and Broadwell-EP B0/M0/R0

CPU microcode MEF406F1_0B00002A to address 'Spectre' variant 2 (CVE 2017-5715) security issue.

2. Updated BIOS version to 3.0a.

3. Updated SATA RAID OPROM/EFI driver to RSTe PreOS v4.7.0.1014.

4. Updated Intel Server Platform Services 3.1.3.50 for Grantley Refresh Platforms.

5. Removed support for using Ctrl+home to trigger recovery.

6. Changed Memory correctable threshold to 100 and enabled Cloaking for Broadwell CPU E5-26xx SKU.

7. Updated BIOS ACM 3.1.1 PW and SINIT ACM 3.1.1 PW.

8. Added BBS reset function to SmcOobLoadBiosDefault().

9. Changed tCCD_L Relaxation default to 1 and changed string from Enabled to Auto.

10. Appended VPD - VB tag in VPD-W Tag(0x91) area.

11. Updated Broadwell-EP RC 4.3.0 PLR11 release.

12. Added SumBbsSupportFlag into DAT file.

13. Updated new MRC error log definition.

14. Enabled OA1_SUPPORT to fix inability to modify OEM Data by AMIBCP.exe.

15. Added Intel SPI vulnerability patch for Grantley.

16. Added "SMBIOS Preservation" Enabled/Disabled item for flash recovery.

17. Displayed setup item "ACS Control" to Enable/Disable PCIe Access Control Services Extended Capability.

18. Implemented SMC Recovery Flash Boot Block feature.

19. Fixed problem of system resetting or hanging after Watch Dog function is enabled during BIOS update.

20. Fixed inability to get correct Memory CECC DIMM location via SD5.