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White Paper

LSTC LS-DYNA® Performance on Supermicro BigTwin™ and AMD EPYC™

Balanced compute resources, memory bandwidth, and network bandwidth deliver outstanding performance and scalability for popular crash simulation software Executive Summary

Executive Summary

LSTC LS-DYNA®: Simulating complex real-world problems

Livermore Software Technology Corporation's (LSTC) LS-DYNA® is a general-purpose finite element program capable of simulating complex real-world problems. It is widely adopted by the automobile, aerospace, construction, military, manufacturing, and bioengineering industries.

High Density, Maximized Value

Compute requirements are increasing, datacenter space is not. Supermicro's innovative BigTwin™ design, powered by AMD's EPYC processors, offer incredible core density with a rich feature set. Innovative server design meets innovative CPU architecture to drive new levels of value in the datacenter.

Conclusion

FEA workloads are demanding and require a balance of memory bandwidth, floating-point performance, and network IO. AMD EPYC processors provide exceptional memory bandwidth and floating-point performance, giving organizations the ability to choose the right balance of scalability and density for their workloads.

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Supermicro BigTwin™ : Where performance meets efficiency for HPC applications

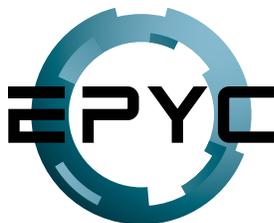
Performance: Support the highest performance AMD® EPYC™ processors for up to 64 cores / 128 threads, up to 2TB of DDR4 memory, and up to 6 hot-swap All-Flash NVMe/SAS3/ SATA3 drives per node for the most demanding workloads.

Density: Incredibly high density with up to 4 hot swappable nodes in a 2U form factor with flexible and robust IO options--1G, 10G, 25G, or 100G Ethernet or 100G InfiniBand, and up to 2 additional low-profile PCI-E 3.0 x16 expansion slots per node.

Efficiency: Designed with power and cost efficiency in mind, the BigTwin reduces power consumption with shared cooling and power design, leveraging redundant 2600W/2200W high efficiency (96%) power supplies. (Full redundancy based on configuration and application load)



AMD EPYC: The right choice for Computer Aided Engineering

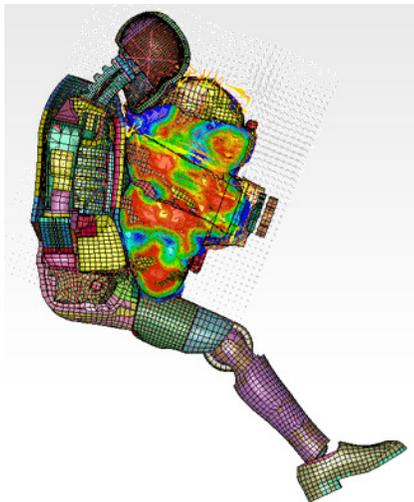


Designed from the ground up for a new generation of solutions, AMD EPYC implements a philosophy of choice without restriction. Choose the number of cores and sockets that meet your needs without sacrificing key features like memory and I/O.

Each EPYC processor can have from 8 to 32 cores with access to incredible amounts of I/O and memory regardless of the number of cores in use, including 128 PCIe lanes, and access to 2 TB of high speed memory per socket across 8 memory channels.

The EPYC Advantage: AMD EPYC server processors offer up to 8 memory channels of DDR4-2666 per CPU, yielding exceptional memory bandwidth.

The EPYC Advantage: Performance - The AMD EPYC processor brings new balance to the datacenter. The highest core count yet in an AMD x86-architecture server processor, large memory capacity, memory bandwidth and I/O density are all brought together in the right balance to help performance reach new heights.



AMD EPYC for Finite Element Analysis

Memory bandwidth is a critical factor in maximizing performance of explicit Finite Element Analysis (FEA) workloads. AMD EPYC server processors' exceptional memory bandwidth ensures that you get the most out of your system, minimizing execution time and increasing overall utilization of your deployment.

Many High-Performance Compute (HPC) workloads require you to balance performance vs per-core license costs to manage your overall cost. AMD EPYC processors offer a consistent set of features across the product line, allowing users to optimize the number of cores required for their workloads without sacrificing features, memory channels, memory capacity, or I/O lanes. Whether you need 8, 16, 24, or 32 physical cores per socket, you will have access to 8 channels of memory per processor across all EPYC server processors.

As workloads demand more processor cores, the communications between processor cores becomes critical to efficiently solving the complex problems faced by customers. As cluster sizes increase, communication requirements between nodes rises quickly and can limit scaling at large node counts. AMD and LSTC have collaborated to offer solutions for FEA workloads enabling exceptional performance and low implementation costs.

LSTC LS-DYNA®

LS-DYNA® is a general-purpose multi-physics, finite element analysis program capable of simulating complex real-world problems. It is used by the automotive, aerospace, construction, military, manufacturing, and bioengineering industries.

LS-DYNA® is widely used by the automotive industry to analyze vehicle designs. LS-DYNA® accurately predicts a car's behavior in a collision and the effects of the collision upon the car's occupants. With LS-DYNA®, automotive companies and their suppliers can test car designs without having to tool or experimentally test a prototype, thus saving time and expense.

AMD and LSTC have continued their partnership, now certifying LS-DYNA® on AMD EPYC-based systems beginning with LS-DYNA® version R9.3.0.

The EPYC Advantage: Collaboration between AMD and LSTC offers high performance and scalability for Finite Element Analysis (FEA) workloads. Customers across automotive, aerospace, construction, military, manufacturing, and bioengineering industries can benefit from the combination of AMD and LSTC.

Performance Testing

LS-DYNA[®] uses a standard set of automotive crash simulation models to measure performance. These models are specifically created to reflect real-world workloads to give a standard basis of comparison across various computer systems and architectures.

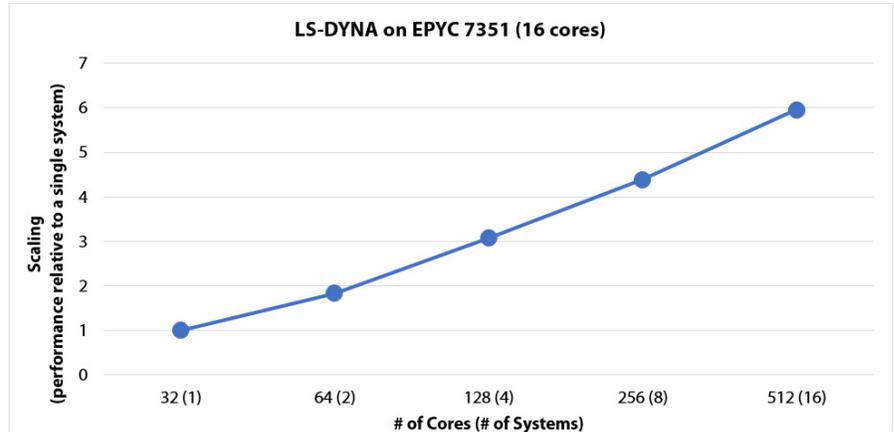
The performance and scalability results shown in this document are using the “Car2Car” model available at TopCrunch.org. These runs simulate the first 120ms of a head-on collision between two vehicles. While this model is relatively small (2.4 million elements) compared to today’s production workloads, it provides a standard baseline for comparing cluster-level performance and scalability of LS-DYNA[®]. Details of the model can be found at: http://topcrunch.org/benchmark_problems.sfe

Tested Hardware/Software configuration

Compute Nodes	
Servers	Supermicro BigTwin™ AS2123BT-HNC0R
CPUs	2 x EPYC 7351 -OR- 2x EPYC 7451
Cores	16 per socket / 32 cores per node
Memory	256GB Dual-Rank DDR4-2666
NIC	Mellanox ConnectX-5 EDR 100Gb Infiniband x16 PCIe
Storage: OS	1 x 256 GB NVMe
Storage: Data	1 x 1 TB NVMe
Software	
OS	RHEL 7.5 (3.10.0-862.el7.x86_64)
Mellanox OFED Driver	MLNX_OFED_LINUX-4.3-3.0.2.1 (OFED-4.3-3.0.2)
MPI Version	Platform MPI (platform_mpi-09.01.04.03)
LS-DYNA R9.3.0	ls-dyna_mpp_s_R9_3_0_x64_redhat54_ifort131_sse2_platformmpi
Network	
Switch	Mellanox EDR 100Gb/s Managed Switch (MSB7800-ES2F)
Configuration Options	
BIOS Setting	SMT=OFF, Boost=ON, Determinism Slider = Power
OS Settings	Transparent Huge Pages=ON (Default), Swappiness=0, Governor=Performance

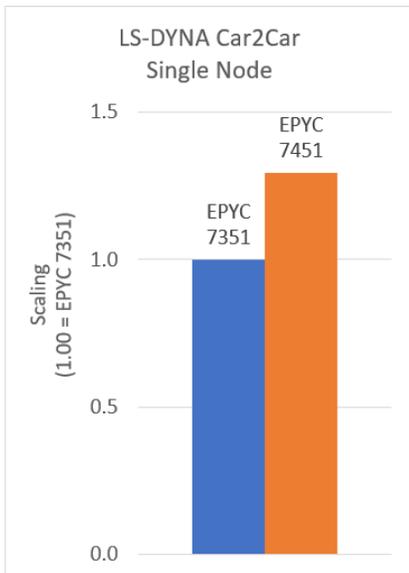
512-core (16-node) Scaling of EPYC 7351

The results below show scaling of a 16-node cluster of dual-socket, EPYC 7351-based systems. Each EPYC 7351 has 16 cores with a base frequency of 2.4 GHz and a boost frequency of 2.9 GHz. Each system has a total of 16 channels of dual-rank DDR4-2666 memory, 8 channels per processor. The scaling metric below represents cluster performance relative to the performance of a single system.



More Bandwidth Allows More Cores per System

FEA workloads are complex and require finding the right balance of floating-point performance, memory bandwidth, and network bandwidth. Many FEA clusters use 16-core processors to balance the memory, IO, and floating-point performance of each node against the communication demands between the nodes. 8 lanes of memory bandwidth on EPYC server processors tilts the balance of system performance. More bandwidth per system means more bandwidth is available to allocate across more cores, allowing more cores to be efficiently added per system.



As demanding FEA workloads scale-out to more threads, inter-process communication requirements can increase dramatically. Moving more of those threads into each system shifts more of the inter-process communication to happen within each node, driving higher per-system performance and density. Whether you are scaling-out to higher node-counts, or driving more density into your clusters, AMD EPYC-based Supermicro BigTwin™ servers gives you more levers to tilt the performance balance your way. This provides new opportunities for more density in your datacenter, even for demanding FEA workloads.

Conclusion

FEA workloads are demanding and require a balance of memory bandwidth, floating-point performance, and network IO. AMD EPYC processors provide exceptional memory bandwidth and floating-point performance, giving organizations the ability to choose the right balance of scalability and density for their workloads.

LSTC LS-DYNA® Finite Element Analysis (FEA) application is architected to deliver accuracy, performance, and scalability. The automotive industry relies up LS-DYNA® to accurately simulate cars' behavior in collisions, allowing increased safety, reduced development costs, and quicker time to production.

For More Information

Together, AMD, Supermicro, and LSTC empower the development of faster, more accurate Finite Element Analysis simulations running on more cost-effective clustered systems.

- For more information about AMD's EPYC line of processors visit: <http://www.amd.com/epyc>
- For more information about Supermicro's AMD EPYC-based servers, visit: <http://www.supermicro.com/epyc>
- For more information about LSTC visit: <http://www.lstc.com>

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About Super Micro Computer, Inc.

Supermicro® (NASDAQ: SMCI), the leading innovator in high-performance, high-efficiency server technology is a premier provider of advanced server Building Block Solutions® for Data Center, Cloud Computing, Enterprise IT, Hadoop/Big Data, HPC and Embedded Systems worldwide. Supermicro is committed to protecting the environment through its “We Keep IT Green™” initiative and provides customers with the most energy-efficient, environmentally-friendly solutions available on the market.

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