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Super Micro Computer, Inc.
980 Rock Avenue
San Jose, CA 95131 USA
www.supermicro.com

White Paper

Ansys® LS-DYNA® Performance on Supermicro BigTwin™ and AMD EPYC™ Processors

Balanced compute resources, memory bandwidth, and network bandwidth deliver outstanding performance and scalability for popular crash simulation software

Executive Summary

Ansys® LS-DYNA®: Simulating complex real-world problems

Ansys® LS-DYNA® is a general-purpose finite element analysis program capable of simulating complex real-world problems. It is widely adopted by the automobile, aerospace, construction, military, manufacturing, and bioengineering industries.

High Density, Maximized Value

Compute requirements are increasing, while datacenter space is not. Supermicro's innovative BigTwin™ family of servers, powered by AMD EPYC processors, offer incredible core density with a rich feature set. Innovative server design meets innovative CPU architecture to drive new levels of value for the datacenter.

Conclusion

FEA (Finite Element Analysis) workloads are demanding and require a balance of memory bandwidth, floating-point performance, and network IO. Supermicro BigTwin, empowered by AMD EPYC processors, provide exceptional memory bandwidth and floating-point performance, offering organizations the benefit of the right balance between scalability and density for their workloads.

Supermicro BigTwin™: Where performance meets efficiency for HPC applications

Performance: Supports the high-performance AMD EPYC™ processors for up to 64 cores/128 threads, up to 4TB of DDR4 memory, and up to 6 hot-swap drives (4 All-Flash NVMe and 2 SATA3) per node for the most demanding workloads.

Density: Incredible high-density with up to 4 hot-swappable nodes in a 2U form factor provides flexible and robust IO options – 1G, 10G, 25G, or 100G Ethernet or 100G InfiniBand, and up to 2 additional low-profile PCI-E 4.0 x16 expansion slots per node.

Efficiency: Designed with power and cost efficiency in mind, BigTwin reduces power consumption with shared cooling and power design, leveraging redundant 2600W/2200W high-efficiency (96%) power supplies. (Full redundancy based on configuration and application load)

AMD EPYC

Processors for HPC

AMD EPYC 7Fx2 processors bring high frequencies and very high ratios of cache per core to the second generation EPYC family of processors. EPYC 7Fx2 processors build on the large memory capacity, extreme memory bandwidth and massive IO of the 2nd Generation EPYC family to deliver exceptional HPC workload performance.

The EPYC Advantage: Performance - The AMD EPYC processor brings new balance to the datacenter. The highest core count yet in an AMD x86-architecture server processor, large memory capacity, memory bandwidth and I/O density are all brought together in the right balance to help performance reach new heights.

High Frequency

Many HPC applications scale very well with frequency. EPYC 7Fx2 series processors offer both base and boost frequencies up to 500MHz faster than the current EPYC 7002 series models enabling significant per-core performance.

High Cache per Core

The 16-core EPYC 7F52 and 8-core EPYC 7F32 processors each boast 16MB of cache for each core. The 24-core EPYC 7F72 processor offers 8MB of cache per-core.

Model	Cores	Base Freq (GHz)	Base Freq (Up to)*	Cache (MB)
EPYC 7F72	24	3.2 GHz	3.7 GHz	192
EPYC 7F52	16	3.5 GHz	3.9 GHz	256
EPYC 7F32	8	3.7 GHz	3.9 GHz	128

* Max boost for AMD EPYC processors is the maximum frequency achievable by any single core on the processor under normal operating conditions for server systems.

A high ratio of cache per core helps feed data into HPC applications using very high-speed cache memory.

Single-Node Performance: EPYC 7F52 vs. EPYC 7351*

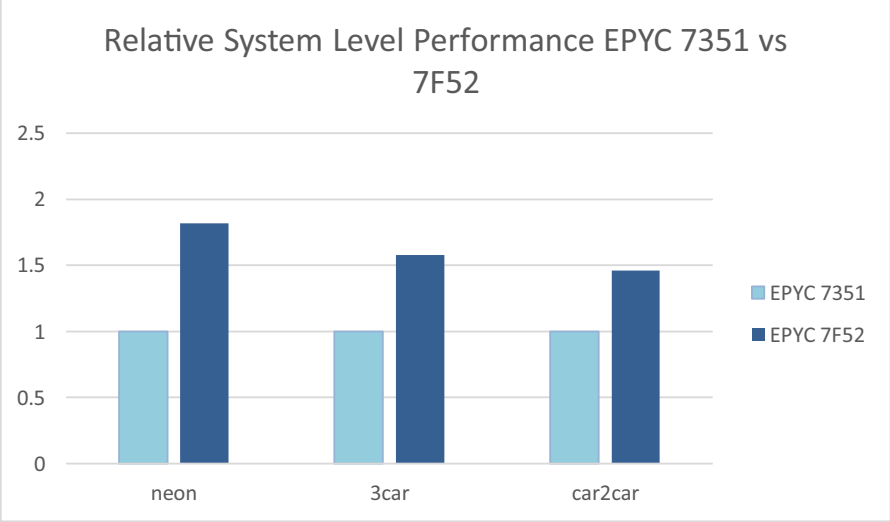

Figure 1. shows the outstanding system level performance of the 16-core AMD EPYC 7F52 CPUs (i.e. up to 70% gain), when upgraded from the 16-core AMD EPYC 7351 CPUs Additional details are available on the April 2020 AMD EPYC document: [Maximizing Ansys LS-DYNA Performance with AMD EPYC 7Fx2 Processors]

SUPERMICRO BIGTWIN ADVANTAGES:

- **Supermicro BigTwin PowerStick Design**
- **Supermicro SIOM – Most Flexible, Cost-Optimized Server I/O**
- **Resource Saving for Best Efficiency and TCO**

A fully tuned BigTwin server coupled with EPYC 7F52 series processors showed on average a 56% performance advantage across the standard LS-DYNA benchmarks.

Scalability

With leadership architecture, 2nd Gen EPYC Series Processors demonstrate very high scalability for HPC applications by supporting 8 channels of memory per processor and PCI-E 4.0.

Ansys® LS-DYNA®

Ansys® LS-DYNA® is a general-purpose multi-physics, finite element analysis program capable of simulating complex real-world problems. It is used by the automotive, aerospace, construction, military, manufacturing, and bioengineering industries.

Ansys® LS-DYNA® is widely used by the automotive industry to analyze vehicle designs. Ansys® LS-DYNA® accurately predicts a vehicle's behavior in a collision and the effects of the collision upon the vehicle's occupants. With Ansys® LS-DYNA®, automotive companies and their suppliers can test vehicle designs without having to tool or experimentally test a prototype, thus saving valuable time and expense.

Supermicro, AMD, and Ansys have continued their partnership, now certifying Ansys® LS-DYNA® on Supermicro BigTwin AMD EPYC based systems beginning with Ansys® LS-DYNA® version R9.3.0.

BigTwin Performance Testing

Supermicro BigTwin incorporating Ansys® LS-DYNA®uses a standard set of automotive crash simulation models to measure performance – the time taken for a job to finish. These models are specifically created to reflect real-world workloads.

The performance and scalability results shown in this document utilize the "Car2Car" model available at TopCrunch.org. These runs simulate the first 120ms of a head-on collision between two vehicles. While this model is relatively small (2.4 million elements) compared to today's production workloads, it provides a standard baseline for comparing cluster-level performance and scalability of Ansys® LS-DYNA®. Details of the model can be found at: http://topcrunch.org/benchmark_problems.sfe

For More Information

Together, AMD, Supermicro, and LSTC empower the development of faster, more accurate Finite Element Analysis simulations running on more cost-effective clustered systems.

- For more information about AMD's EPYC line of processors visit: http://www.amd.com/epyc
- For more information about Supermicro's AMD EPYC-based servers, visit: http://www.supermicro.com/epyc
- For more information on Maximizing Ansys® LS-DYNA® Performance with AMD EPYC™ Processors, visit here
- For more information about LSTC visit: http://www.lstc.com

Tested Hardware/Software configuration

Compute Nodes	
Servers	Supermicro BigTwin™ AS -2124BT-HNTR
CPUs	2x EPYC 7F72 -OR- 2x EPYC 7F52
Cores	**EPYC 7F52:** 16 cores per socket / 32 cores per node **EPYC 2F72:** 24 cores per pocket / 48 cores per node
Memory	1,024GB Dual-Rank DDR4-2933
NIC	Mellanox CX-6 HDR 200Gb/s x16 PCI-E Gen 4
Storage: OS	1x 960 GB U.2
Storage: Data	1x 1 TB NVMe M.2
Software	
OS	RHEL 7.7 (3.10.0-1062.el7.x86_64)
Mellanox OFED Driver	MLNX_OFED_LINUX-4.7-1.0.0.1
MPI Version	Platform MPI (platform_mpi-09.01.04.03)
LS-DYNA R9.3.0	ls-dyna_mpp_s_R9_3_0_x64_ redhat54_ifort131_sse2_ platformmpi
Network	
Switch	Mellanox EDR 100Gb/s Managed Switch (MSB7800-ES2F)
Configuration Options	
BIOS Setting	BIOS settings: Defaults, plus NPS=NPS4 (7F52), NPS=NPS2 (7F72), SMT = Off, Boost = On, APBDIS=1, Fixed SOC P state=P0, DLWM=off, X2APIC = On, Determinism Slider = Performance, Preferred IO=Enabled
OS Settings	Transparent Huge Pages=disabled, Swappiness=disabled, Governor=Performance

The results below illustrate how the Supermicro BigTwin supporting the AMD EPYC 7F52 processor can be scaled on LS-DYNA OBD-10M. Same scaling can be shown with other benchmarks like Neon, 3cars, Car2car.

Figure 2. Additional details are available on the April 2020 AMD EPYC document: [Maximizing Ansys LS-DYNA Performance with AMD EPYC 7Fx2 Processors]

LS-DYNA Scaling Performance

Building on dominant performances, Supermicro BigTwin, in Figure 2, demonstrates how it scales up linearly through an 8-node configuration.

Conclusion

FEA (Finite Element Analysis) workloads are demanding of system resources and require a balance of memory bandwidth, floating- point performance, and network IO. Supermicro BigTwin empowered by AMD EPYC processors, provides exceptional memory bandwidth and floating-point performance, offering organizations the benefit of the right balance between scalability and density for their workloads.

Supermicro BigTwin incorporating Ansys® LS-DYNA® (FEA) applications is architected to deliver accuracy, performance, and scalability. The automotive industry relies on LS-DYNA® to accurately simulate vehicle behavior in collisions, allowing increased safety, reduced development costs, and quicker time to production.

NOTES

About Super Micro Computer, Inc.

Supermicro®, the leading innovator in high-performance, high-efficiency server technology is a premier provider of advanced server Building Block Solutions® for Data Center, Cloud Computing, Enterprise IT, Hadoop/Big Data, HPC and Embedded Systems worldwide. Supermicro is committed to protecting the environment through its "We Keep IT Green®" initiative and provides customers with the most energy-efficient, environmentally-friendly solutions available on the market.

Learn more at www.supermicro.com

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